# MODULAR REFERENCE DESIGN PLATFORM


January 2008

SONET Aggregation and T/E Carrier Applications Group



XRUM00001

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## 1.0 INTRODUCTION TO ORION

The Orion Modular Reference Design Platform serves to demonstrate Exar's broadband product portfolio solutions and capabilities in Metropolitan Access Networks. The Orion MRDP can showcase viable solutions within the capabilities of Exar's product devices in a multitude of network service applications.


**Orion Platform Target Deployment Applications:**

- **Add Drop Multiplexer (ADM) Devices**
- **Digital Loop Carriers (DLC)**
- **Digital Subscriber Line Access Multiplexer (DSLAM)**
- **SONET/SDH based transmission systems**
- **SONET/SDH based modules**
- **Plesiochronous/PDH Networks**
- **Broadband Cross Connect Systems**
- **Dense Wave Division Multiplexer Termination Equipment**
- **Multi-Service Switches and Routers**
- **Multi-Service Provisioning Platforms**
- **Wireless Broadband Network Base Stations**

### *1.1 ORION Modular Reference Design Platform Features*

The following features are supported on the Orion MRD Platform.

- **Self-Contained Stand Alone Unit**
- **USB 2.0 Compliant GUI Enabled Software Programmable Control**
- **Service Oriented Modular Line Card Flexibility**

This self-contained module may be used as an evaluation and demonstration tool. The GUI Applicaton through the USB interface on a Host Personal Computer can be used to provision and control the use of Exar's product device to showcase it's application's scalability, flexibility, and unique capabilities.

## 2.0 THE ORION PLATFORM

The Orion Modular Reference Design Platform is a stand alone unit consisting of:

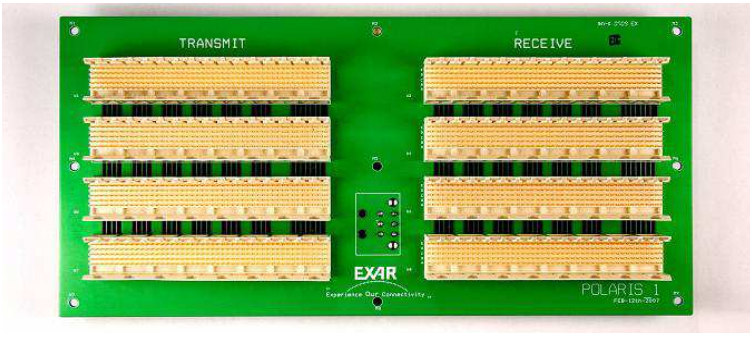
- A Multi-Layer High Density Backplane
- An FPGA based USB 2.0 GUI Enabled Software Common Control Card
- Three Modular Line Card Access Slot
- A Display Polymer Cube Chassis
- A 240V/120V 30W Integrated Power Supply Unit

**FIGURE 1. ORION REFERENCE DESIGN PLATFORM**


### *2.1 The Modular High Density Backplane*

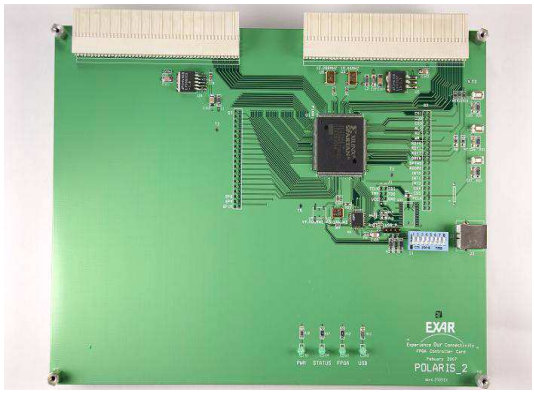
This Modular High Density Backplane has the main function for interconnecting and integrating the reference design line cards and delivering line card access for functionality control. It is the key backbone of the Orion platform providing the necessary cross-connects for operability.

**FIGURE 2. THE MODULAR HIGH DENSITY BACKPLANE**



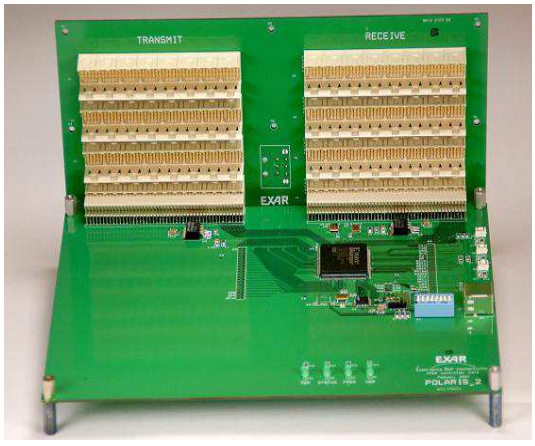
### 2.2 FPGA Based USB 2.0 GUI Enabled Software Common Control Card

The Common Control Card has the specific function of provisioning the populated reference design cards. The FPGA provides direct access to the microprocessor bus thus enabling a GUI supplied software running on a PC with a USB interface to configure and provision all the elements within the Reference Design Line Cards for demostrating Exar device's key operability and unique capabilities and performance.




### 2.3 Modular Line Card Access Slot

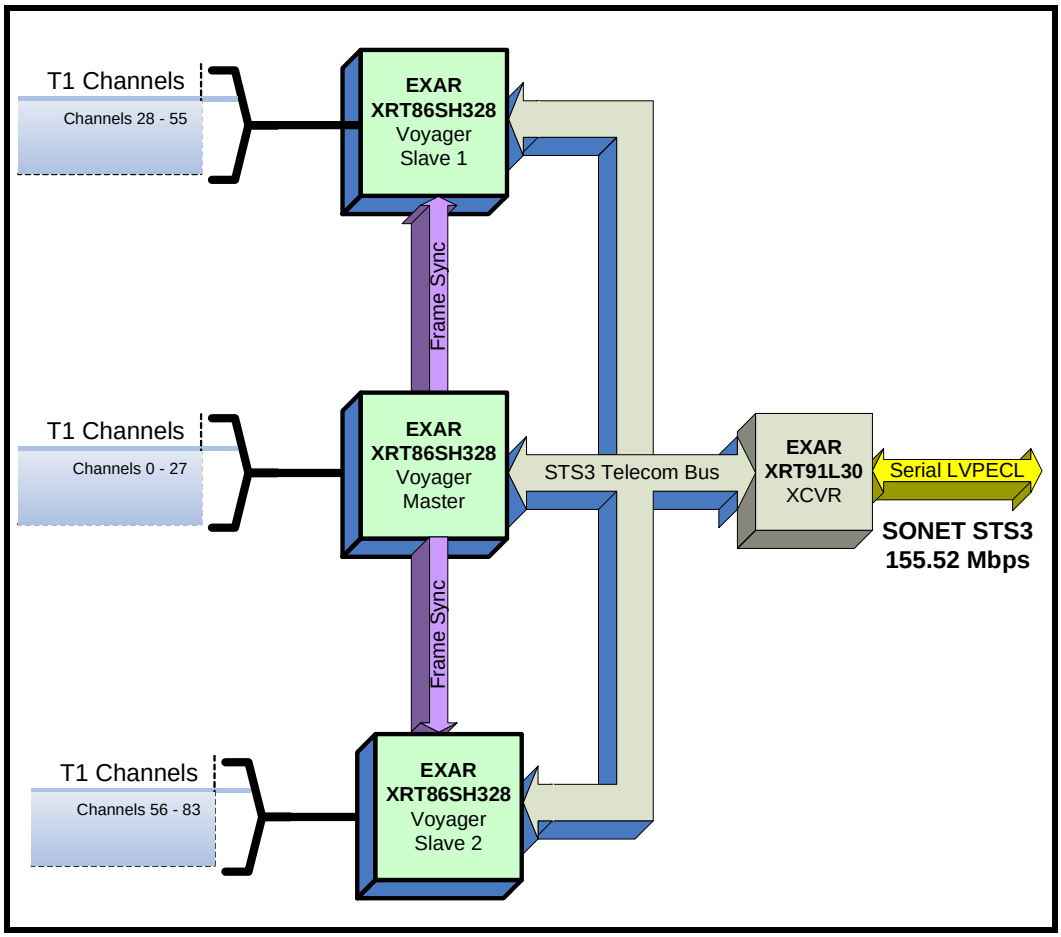
There are three Modular Line Card Access Slot for populating reference design platforms. These slots provide the user scalability and flexibility in choosing design platforms for their specific target applications. Customers can quickly evaluate and validate Exar devices in proven solutions with their intended applications before they ever begin to allocate and develop significant resources in their project. Having the reference design solution before development greatly reduces risk on the customer part in developing new applications for Exar devices while quickly gaining confidence in the product performance and viability. With today's increasingly competitive global market and emerging economical challenges, the platform also serves customers seeking a cost reduction alternative to their existing solutions by having the ability to evaluate Exar devices in exceptional and proven solutions without functional and performance compromise.



## 3.0 THE XRT86SH328/221 TRIPLE VOYAGER REFERENCE DESIGN PLATFORM

The XRT86SH328/221 Triple Voyager Reference Design Platform offers an unmatched high density unique solution packing 84 T1 or 63 E1 channels into VT1.5 tributaries and directly mapping them into SONET/SDH STS3/STM1 data rate. The main elements in the design consists of three XRT86SH328/221 Voyager devices using a common telecom bus operating at 19.44MHz. For optical transmission, the STS3/STM1 telecom bus interface is coupled with the XRT91L30 transceiver and an optical module. Each XRT86SH328/221 devices can map 28 T1 or 21 E1 channels for a total of 84 T1 or 63 E1 channels. The Triple Voyager Design trully demonstrates the XRT86SH328/221 device extraordinary capabilities and delivers high density T1/E1 applications in the market today.

**FIGURE 3. XRT86SH328 TRIPLE VOYAGER BLOCK DIAGRAM**

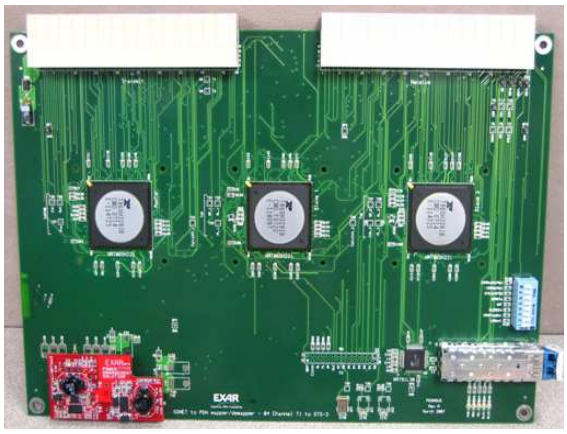



### *3.1 Master vs Slave Mode*

For STM-1 applications, all three devices should be programmed to Slave. The "Master" device will occupy time slot 0 as a slave so that the system provides 2kHz to all three devices. This allows the V1 bytes to be aligned. In this mode, B1 is NOT calculated (see errata).

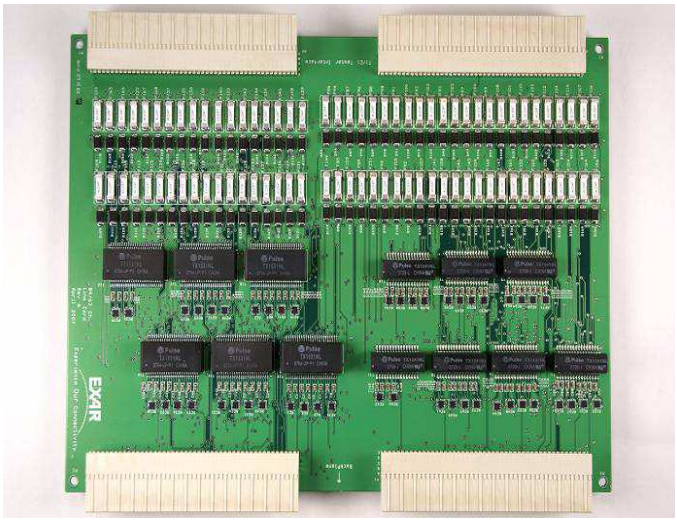
### 3.2 The XRT86SH328/221 Triple Voyager Line Card

The XRT86SH328/221 Triple Voyager Line Card Reference Design Platform exemplifies Exar's lead in telecommunications silicon industry, providing a highly integrated unique STS3/STM1 SONET/SDH solution in high density VT Mapper T1, E1, and J1 applications. Customers implementing Exar's innovative solution can deliver cutting edge products while significantly reducing their cost with the simplification of their Bill of Materials and Board System Design.



### 3.3 The XRT86SH328/221 Triple Voyager T1/E1/J1 Magnetics Line Card

The XRT86SH328/221 Triple Voyager T1/E1/J1 Magnetics Line Card provide access to a density total of 84 T1 or 63 E1 channels. Each of the three XRT86SH328 Voyager device maps 28 T1 or 21 E1 channels.

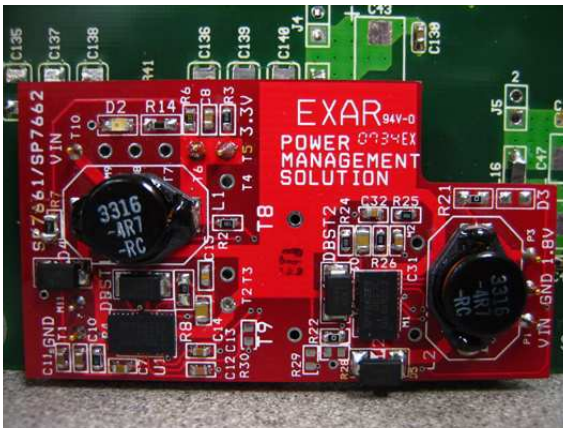


### 3.4 *Exar PowerBlox™ Power Management Solution Reference Design*

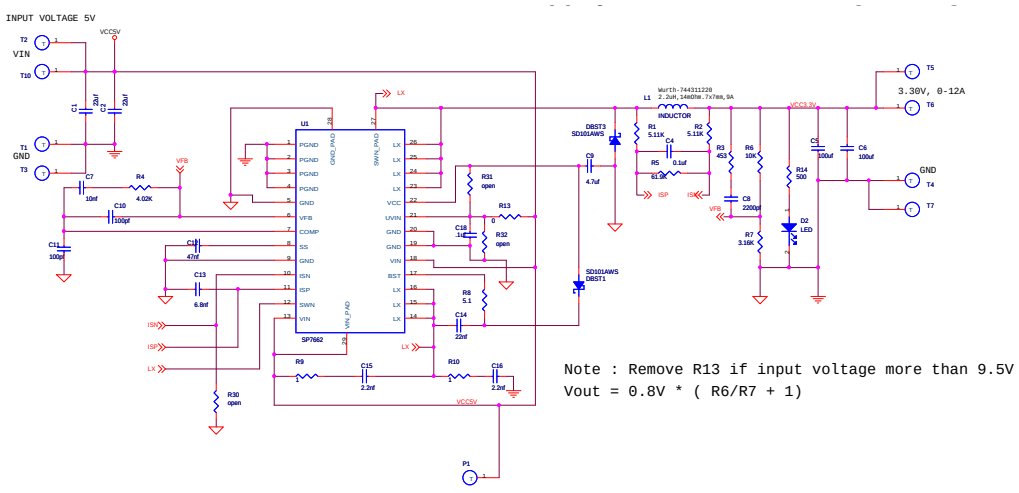
Powering the XRT86SH328/221 Triple Voyager Line Card Reference Design is the Exar's proven PowerBlox™ Power Management Solution. The PowerBlox™ Power Management Solution is compromised of Exar's leading edge SP7662 and SP7663 Buck Regulators. The SP7662 is capable of supplying 12 Amps at 3.3V and the SP7663 can drive up to 6 Amps at 1.8V. The SP7662/SP7663 are synchronous step-down switching regulators optimized for high efficiency. These devices is designed for use with a single 5V(SP7662)/4.75V(SP7663) to 22V single supply or 3V to 22V input if an external Vcc is provided.

The SP7662/SP7663 provides a fully integrated buck regulator solution using a fixed 300/ 600(respectively) kHz frequency, PWM voltage mode architecture. Protection features include UVLO, thermal shutdown, output current limit and short circuit protection. The SP7662 and the SP7663 are available in the space saving DFN package.

PowerBlox™ Power Management Solution




SP7762 Schematic Reference Design



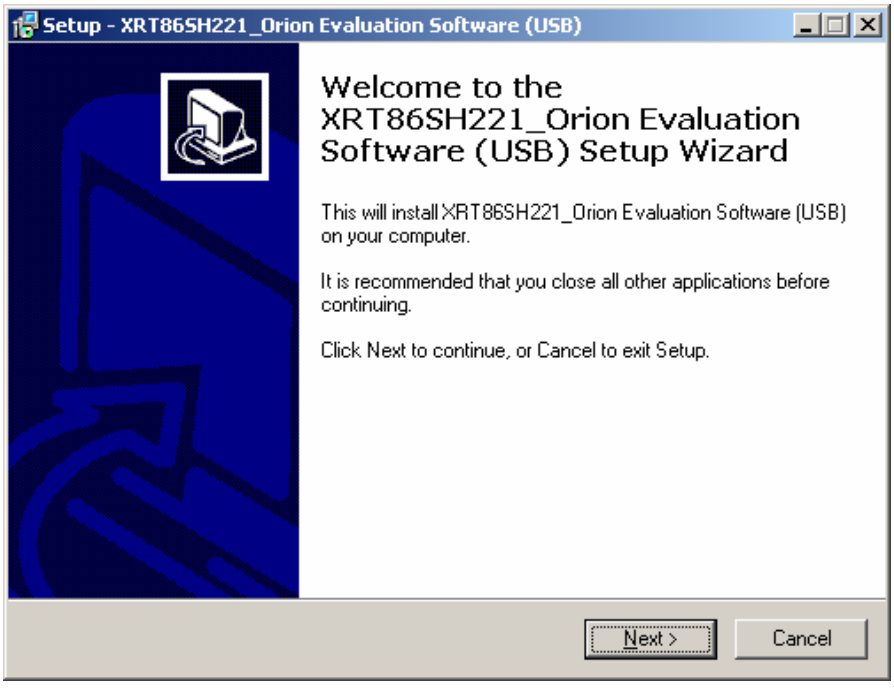
## 4.0 THE XRT86SH221 TRIPLE VOYAGER LITE GRAPHICAL USER INTERFACE

The GUI is intended to allow easy access to configure basic registers in the 3 Voyager Lite devices on the reference design platform.

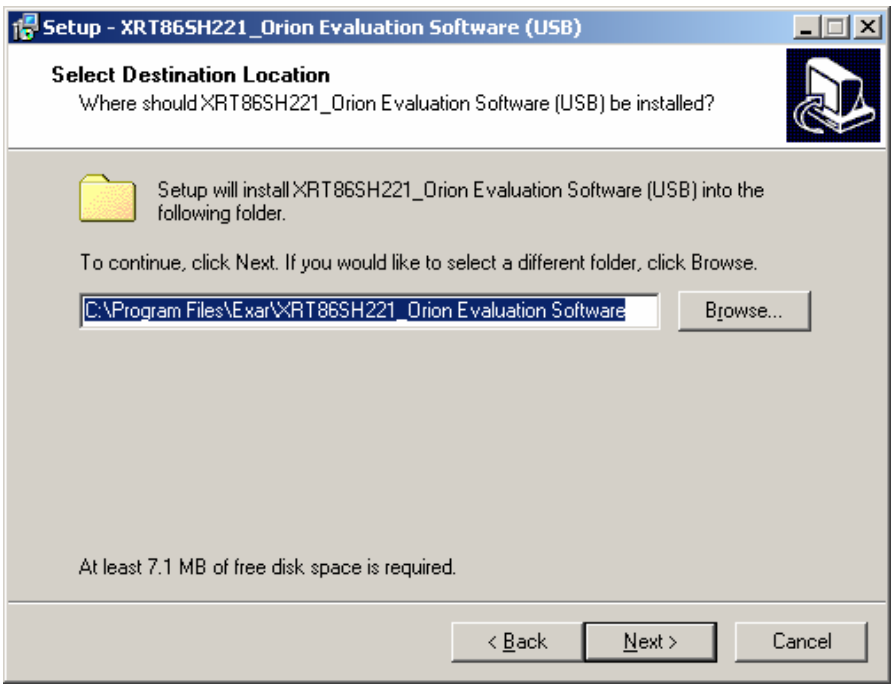
### *4.1 XRT86SH221 Triple Voyager Lite GUI Setup and Installation*

Included in every Orion Modular Reference Design Platform is an Installation file. Located within the contents of the CDROM, the installation filename for the XRT86SH221 Triple Voyager Reference Design Platform is called "***XRT86SH221_Orion EvaluationUSB08022007.exe***". This file will automatically load the Exar USB drivers and install the XRT86SH221 Triple Voyager Reference Design Platform GUI software. However, if the following steps are performed and the board is NOT recognized by the PC, **SEE"MANUALLY LOADING EXAR DRIVERS (IF INSTALLATION IS NOT SUCCESSFUL)" ON PAGE 14.** that describes how to manually load the drivers.

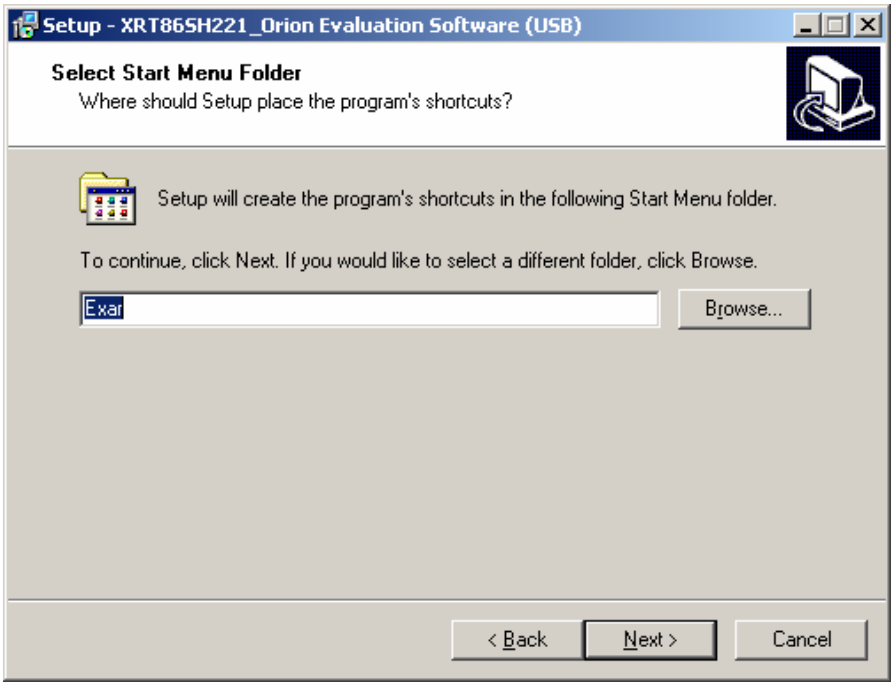
**Step 1** Double Click the "***XRT86SH221_Orion_EvaluationUSB_08022007.exe***" file to bring up the following screen. Click on the **Next>** button.



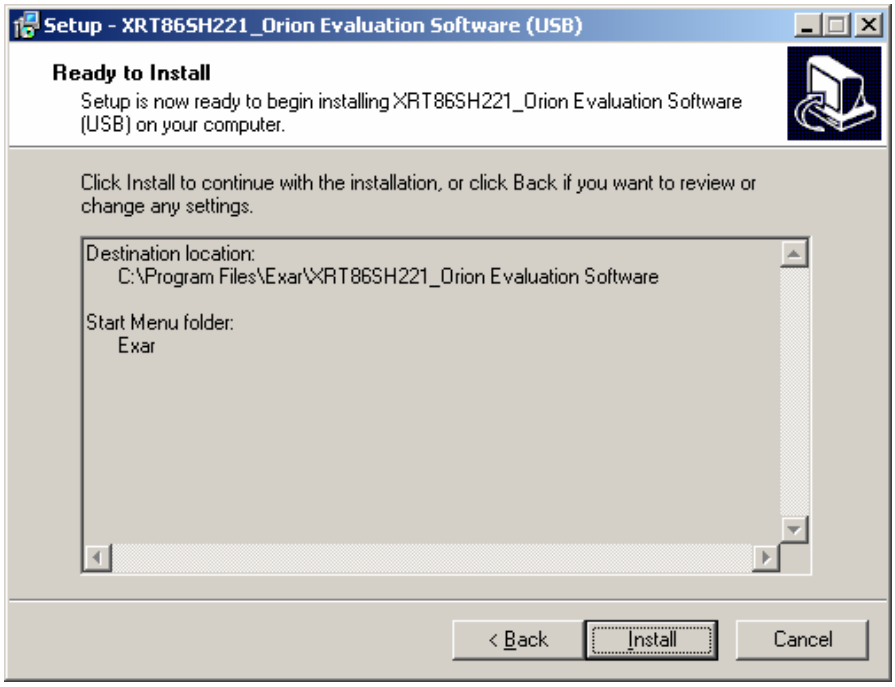
**Step 2** If there are no changes to the installation directory, Click on the **Next >** button to proceed. Otherwise, make the necessary changes and Click on the **Next >** button to proceed.



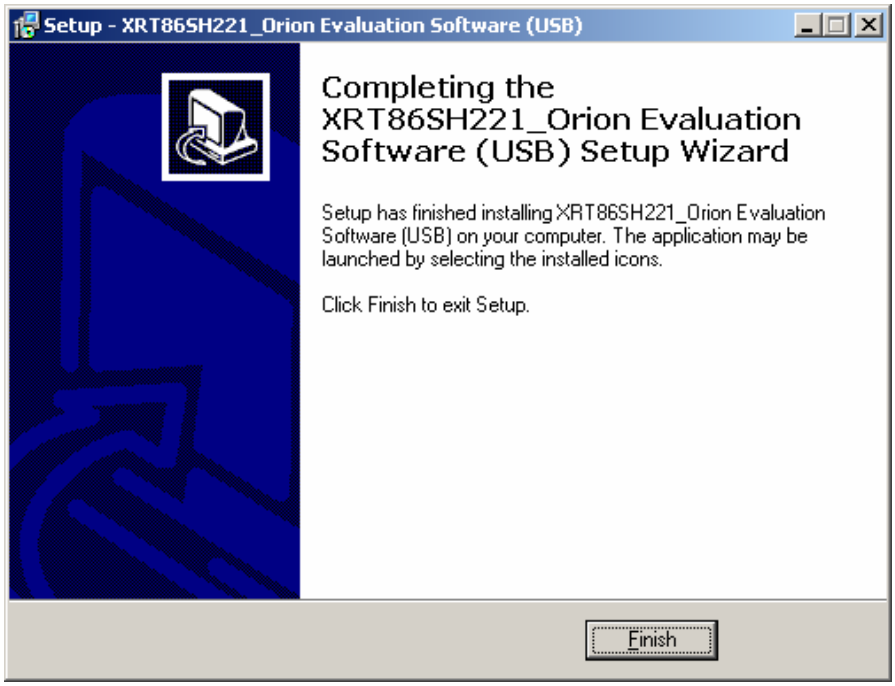

**Step 3** Click the **Next>** button to continue.



**Step 4** Click on the **Install** button to continue installation.



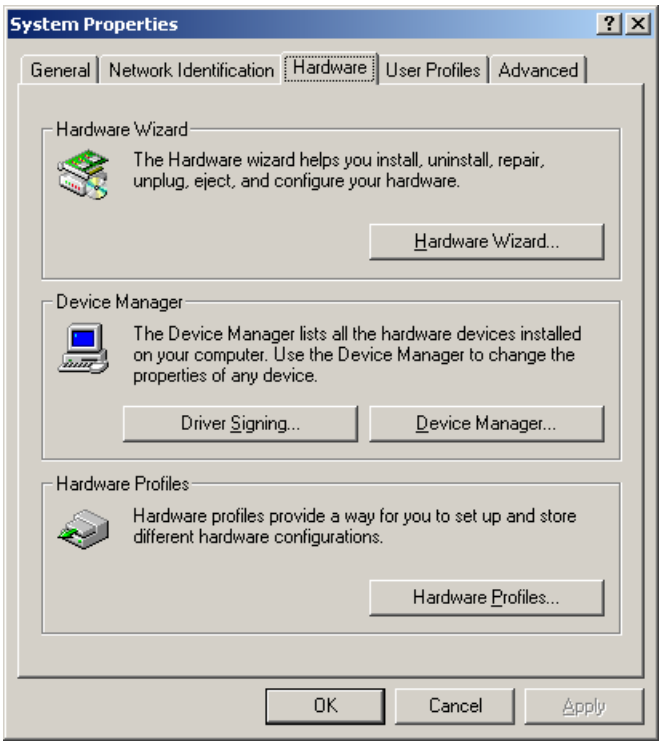

**Step 5** Click on the **Finish** button to complete installation. The Exar USB drivers should be properly installed and ready to go. If so, continue to the next section that describes the Graphical User Interface. If not, see the last step below to manually load the Exar USB Drivers.



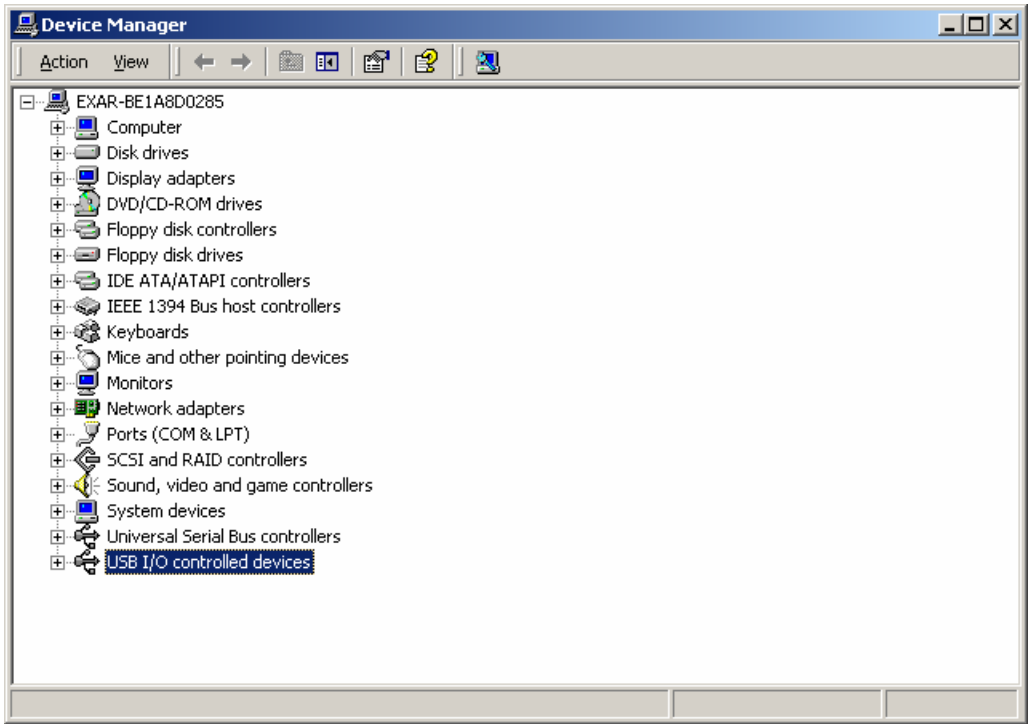
### 4.1.1 Manually Loading Exar Drivers (If Installation is NOT Successful)

If the Evaluation Board is NOT recognized and/or the installation process was NOT successful, most likely there is a driver contention or the driver was not installed in the proper directory from the software. This section describes how to manually load the drivers.

Note: Each Windows operating system may access the System Hardware differently. Therefore, it is not practical to describe this procedure for each OS. However, the key component is usually the Control Panel of the PC. From the Control Panel, you can access the System Properties dialog box. From there, choose the Hardware menu item and go to the Device Manager…



The device Manager will bring up the following dialog box. Choose the USB I/O Controlled Devices, select Exar Device, right click, select properties, select Update Driver, and then follow the directions to choose the driver from the CD or the /Driver directory in the Exar working directory ("C:\Program Files\Exar\3VoyagerLites Evaluation Software" by default).



### *4.2 STARTING THE XRT86SH221 TRIPLE VOYAGER LITE GUI*

The evaluation software allows the user to do the following:

- Configure the XRT86SH221 for proper operation
- Poll current and historical performance status
- Download the FPGA file
- Enable/Disable XRT86SH221 features with the click of a button

#### Initialization of the GUI

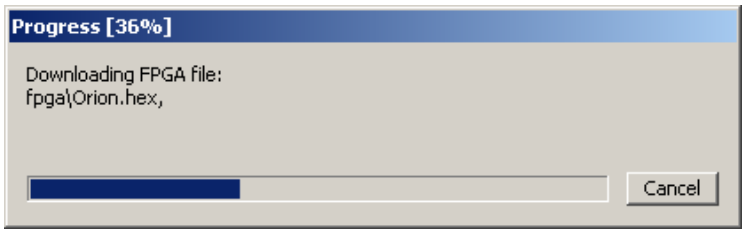
Once the USB Installer program is completed, all files are installed under the directory: "**C:\Program Files\Exar\XRT86SH221_Orion Evaluation Software**" (If the user did not change the default directory for installation).

There are two ways to initialize the GUI:

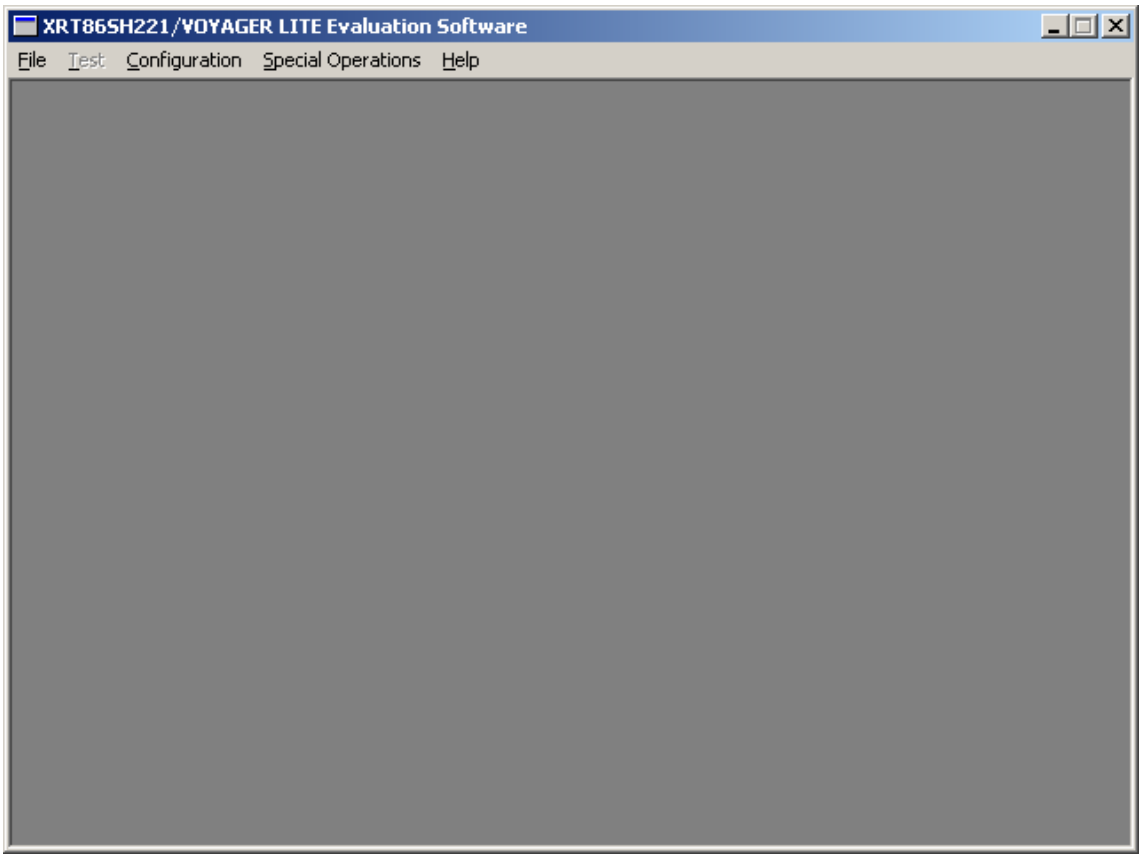
- 1. Double Click the file "3VoyagerLitesGui.exe" under the installed directory.
- 2. Click on the **Start** button then choose **Programs > Exar > XRT86SH221_Orion Evaluation Software > XRT86SH221_Orion Evaluation GUI**. Once the GUI is initiated, the software will download a .hex file from the installed directory automatically. If the downloading fails, the following dialog box will appear.


If there is an error loading the FPGA file, refer to the section that describes "Manually Loading Exar Drivers".

After executing the program, the following dialog box will appear to notify the user that the FPGA file is being downloaded to the on board FPGA.




If the FPGA has been successfully loaded, the following main dialog box will appear.



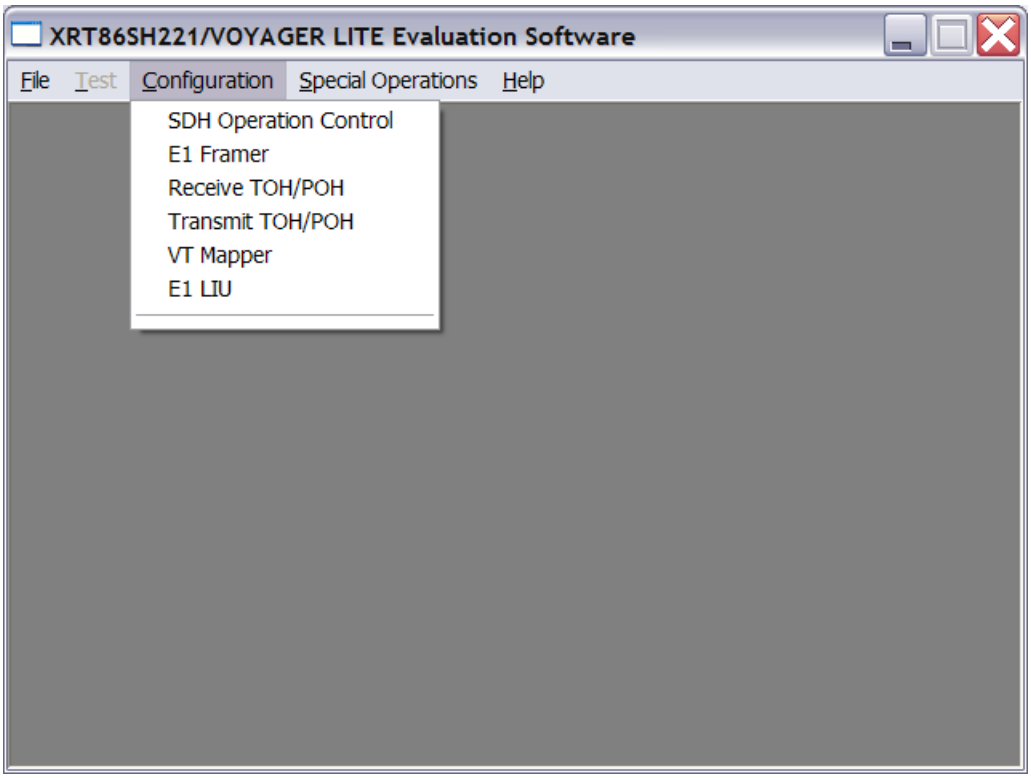
### The Main Dialog Box

There are two main selection items on the tool bar.

1. Configuration
2. Special Operations

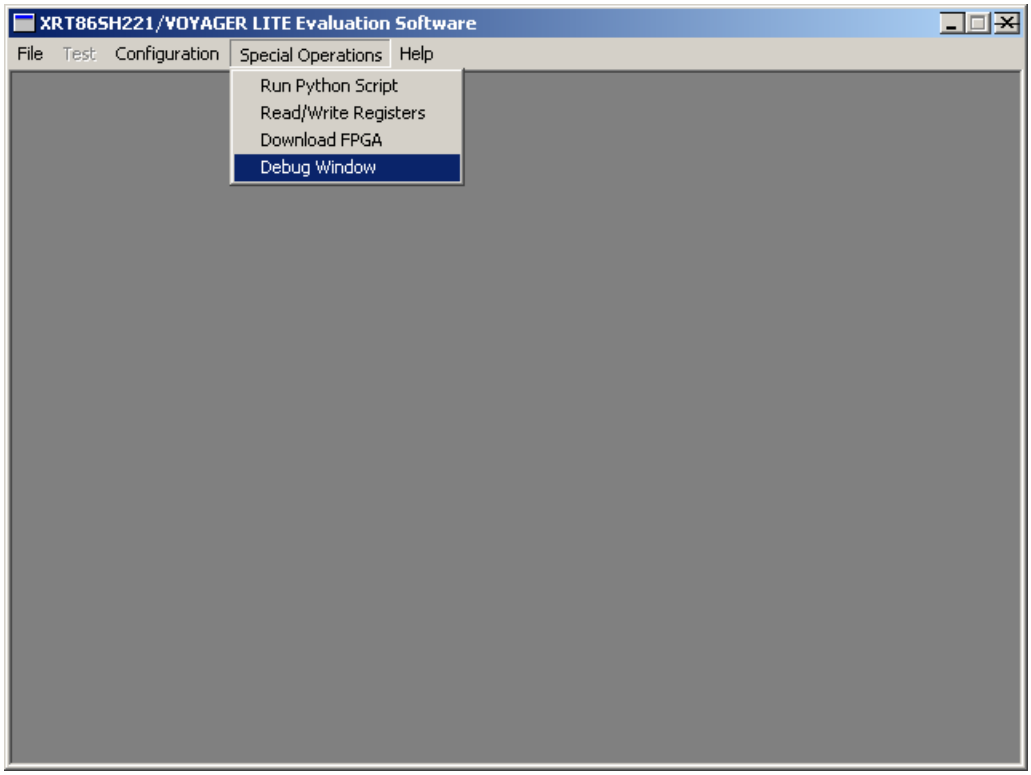
Under the Configuration menu, the following items will appear. You'll have the option to program in each of the three Voyager Lite devices:

- SDH Operation and Control
- E1 Framer
- Receive TOH/POH Blocks
- Transmit TOH/POH Blocks
- VT Mapper
- E1 LIU Registers.



Under the Special Operations menu, the following items will appear. You'll have the option to do one of the following:

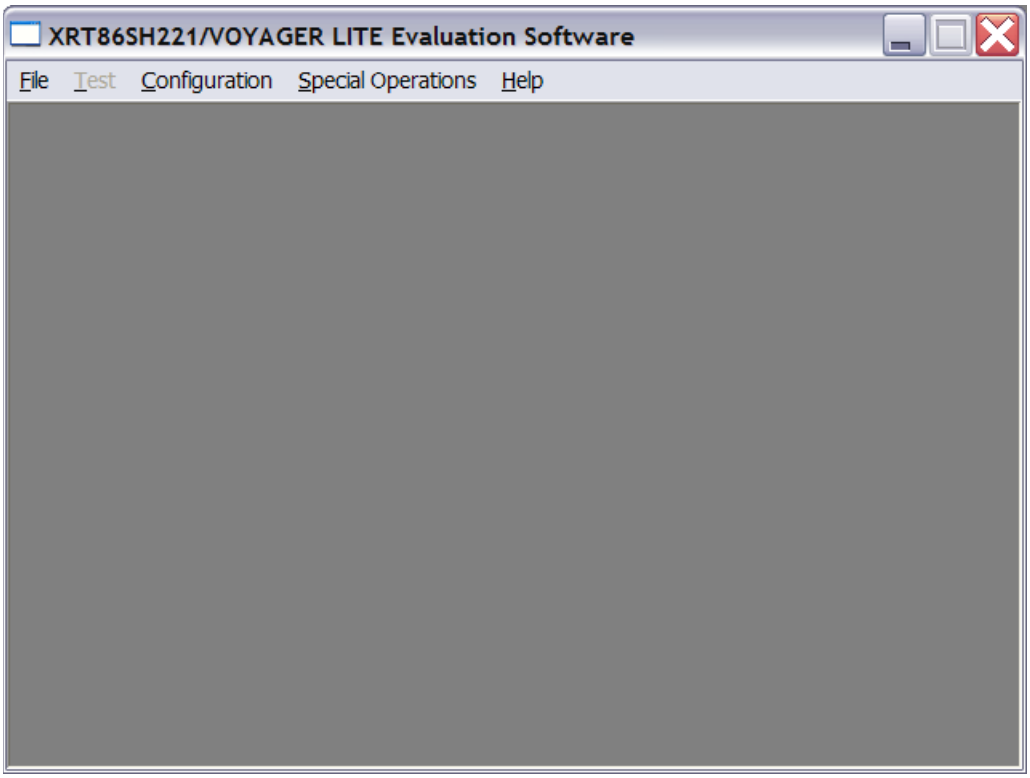
1. Run Python Script (Script Files are Automatically Loaded)
2. Read/Write Registers (Allows Access to a Manual Read or Write)
3. Download FPGA
4. Debug Window (Interactive Tool to Monitor Register Activity)



### *4.3 Using the Evaluation Software*

It is possible to achieve full device functionality through the GUI. The XRT86SH221 and other device features are also accessed and can be enabled or disabled through the main GUI window. Upon each selection, the control pin assertion or software register operation occurs immediately and is displayed in the main GUI window.

Once the FPGA has been successfully programmed, you should see a similar window below. To begin the Triple Voyager Lite Evaluation, Select "Configuration" on the Menu.



### 4.3.1 Operation Control Block

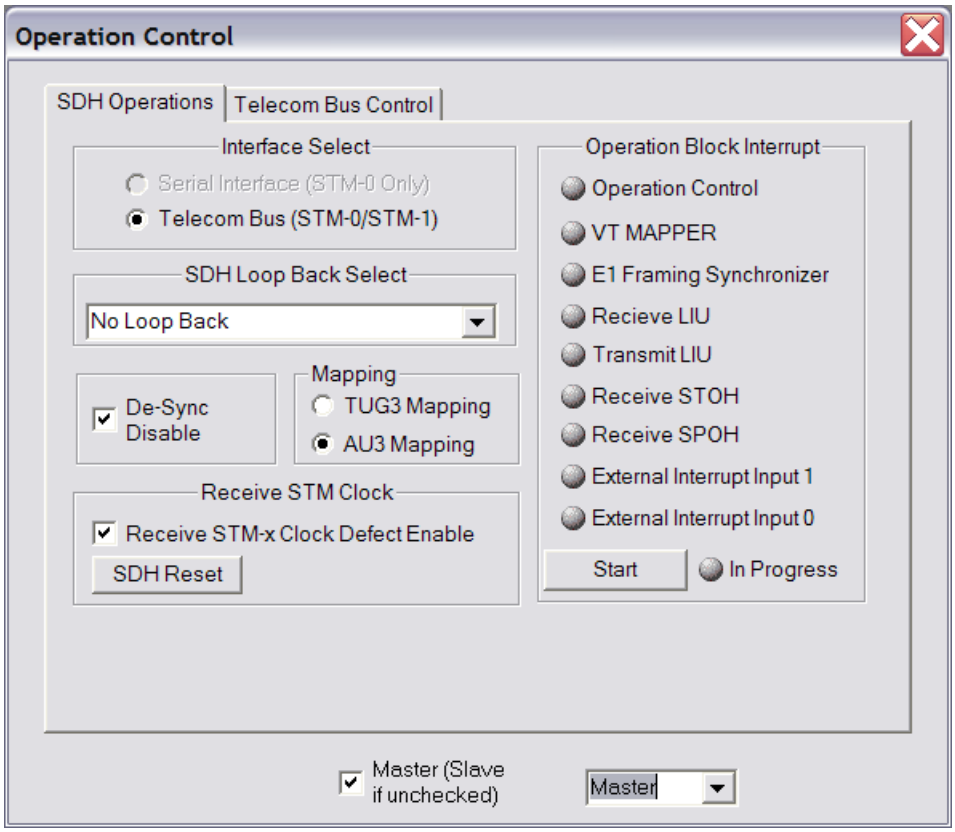
There are two pages in the Operation Control block dialog:

- **SDH Operations**
- **Telecom Bus Control.**

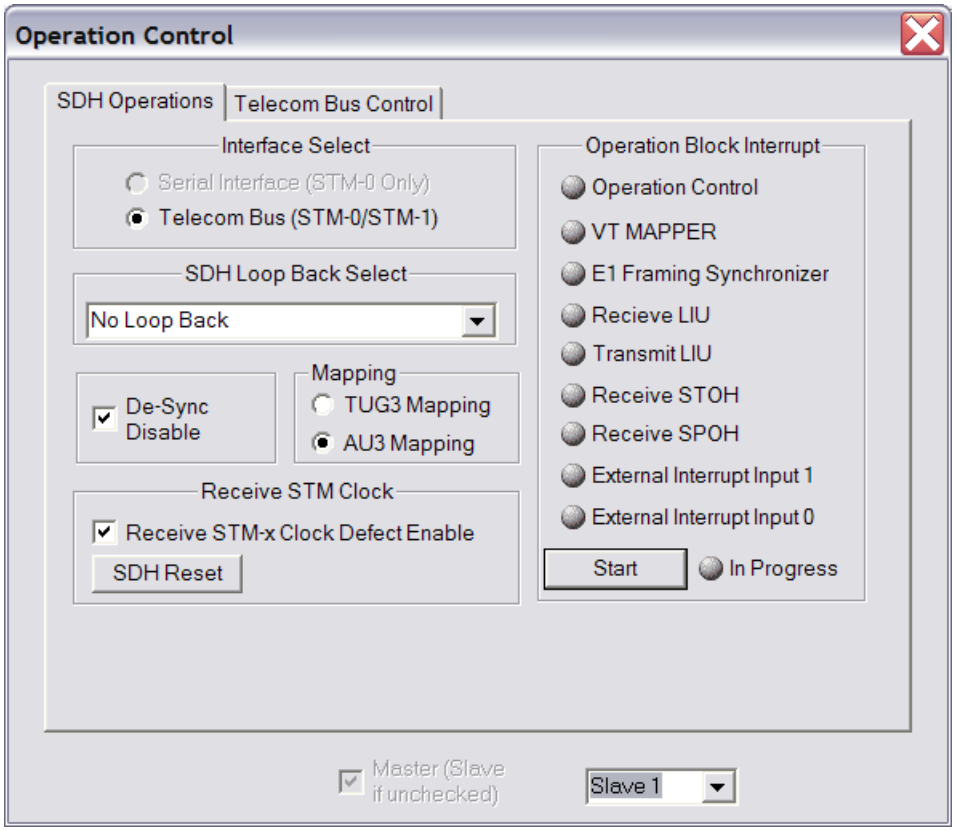
Click on the labeled tabs to switch to the wanted page.

#### *4.3.1.1 SDH Operations*

Selecting "SDH Operation Control" on the drop list, the following window will appear. Each of the three XRT86SH221 are independently accessed and controlled by an "Operation Control" window. All dialog boxes have a pull down menu for specifying which device, Slave 0, Slave 1 or Slave 2, is being controlled by the dialog box. Slave 0 device can also be converted to Master device by clicking the checkbox on the left of the pull down menu. The default "Operation Control" window will automatically select the "Master" device of the three XRT86SH221.



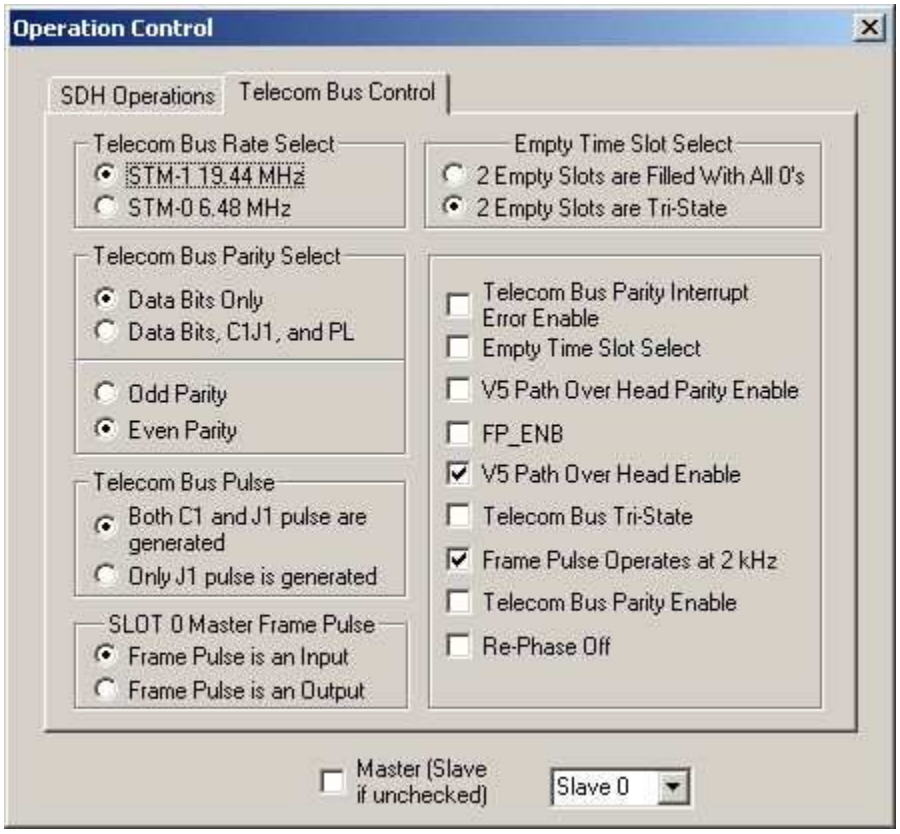
To select and provision the Slave 1 and Slave 2 Voyager Lite device, the user can open multiple windows (a second and a third "Operation Control" window) by Clicking-On "Configuration" on the Menu followed and selecting "SDH Operation Control" on the drop list. Slave 1 or Slave 2 is selected on the Drop Down List near the bottom of the application window.




Status indicators will begin polling upon selecting the Start Poll button and will continue to poll until it is stopped.

#### *4.3.1.2 Telecom Bus Control*

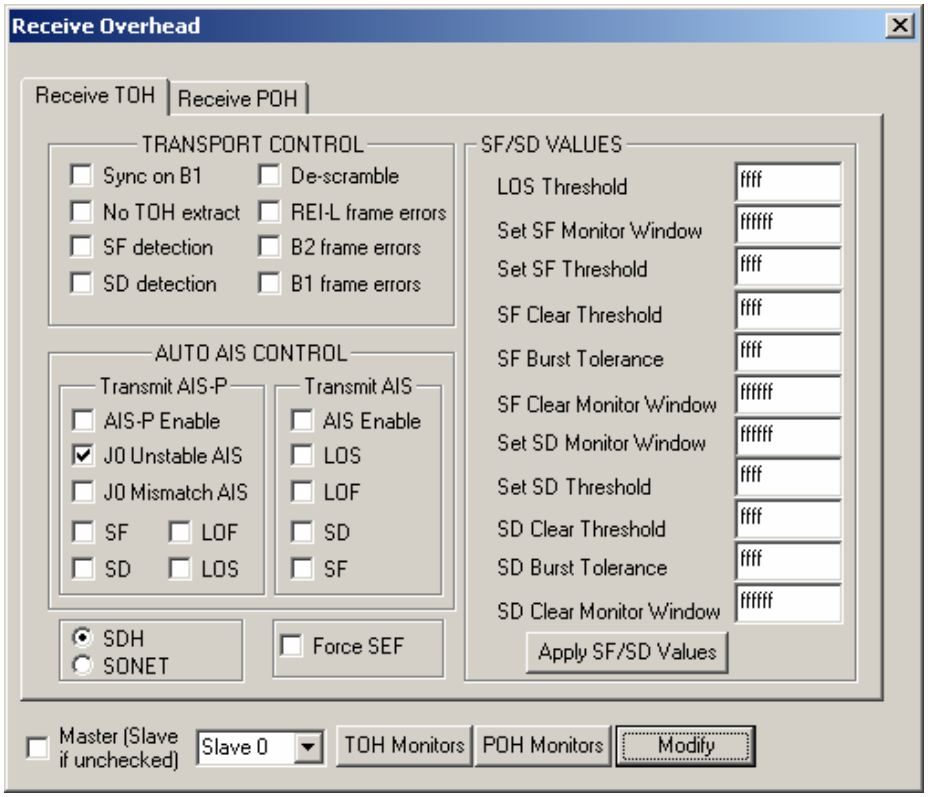
Selecting "Telecom Bus Control" on the drop list, the following window will appear. Again, each of the three XRT86SH221 are independently accessed and controlled by an "Operation Control" window. All dialog boxes have a pull down menu for specifying which device, Slave 0, Slave 1 or Slave 2, is being controlled by the dialog box. Slave 0 device can also be converted to Master device by clicking the checkbox on the left of the pull down menu. The default "Operation Control" window will automatically select the "Master" device of the three XRT86SH221.



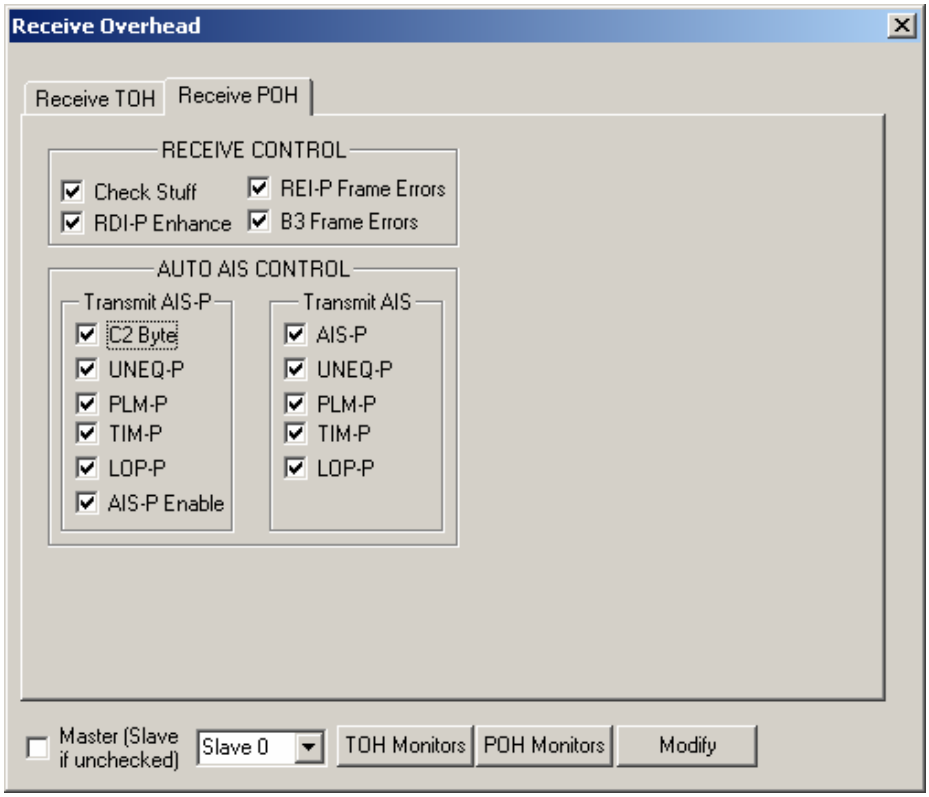
### 4.3.2 Receive SDH Overhead

On the Receive SDH Overhead dialog, the two pages are for Regenerator and Mulitplex Section OH (TOH) and High-Order Path Overhead (POH). There are two buttons, TOH Monitors and POH Monitors, on the bottom of the dialog for displaying status indicators. Click on the two buttons will evoke two separate dialog boxes, which contain all the status indicators.

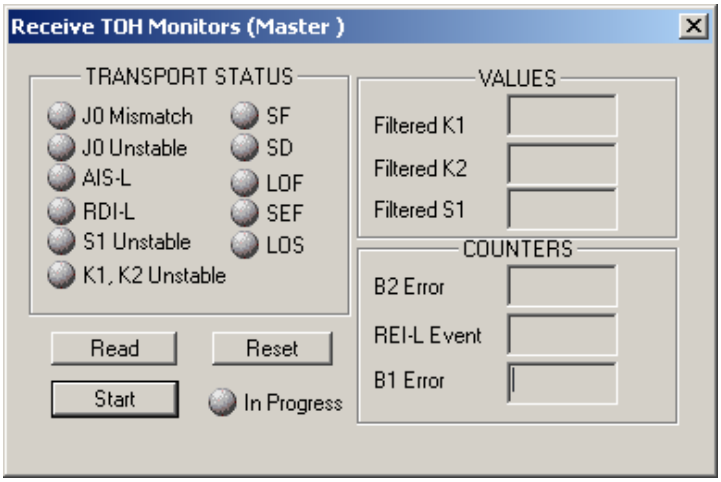
#### *4.3.2.1 Receive Regenerator and Multiplex Section Overhead (Receive TOH)*



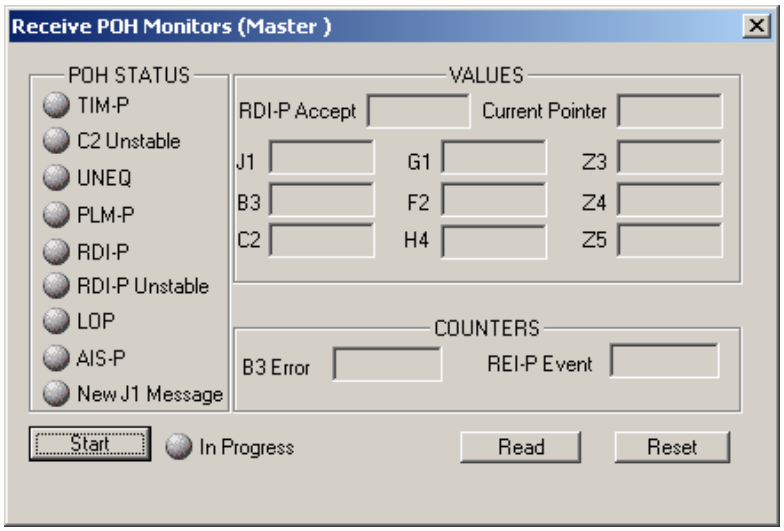
#### *4.3.2.2 Receive High-Order Path Overhead (Receive POH)*




### 4.3.3 Receive Regenerator and Multiplex Section Performance Monitors



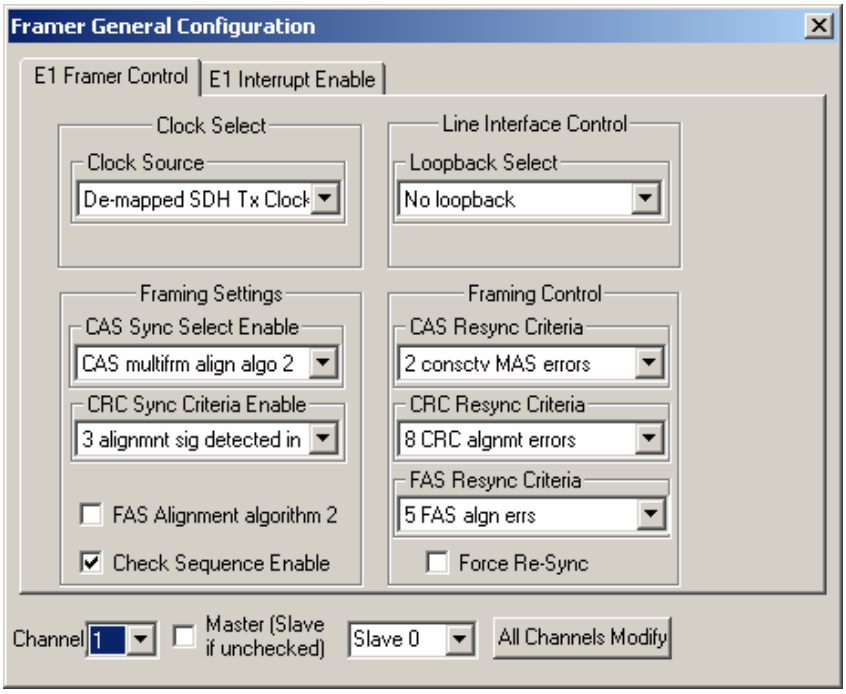
### 4.3.4 Receive High-Order Path Performance Monitors



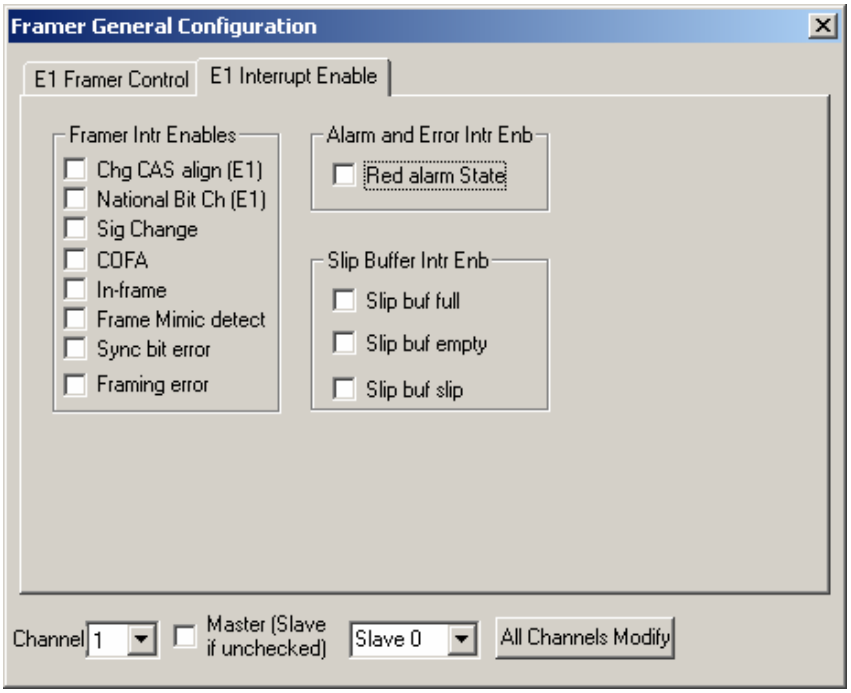

### 4.3.5 E1 Framer General Configuration

The dialog box for framer block also has two pages, E1 Framer Control and E1 Interrupt Enable. The All Channel Modify button is used to modify all channels on the specified board with the same settings on the current dialog box.

#### *4.3.5.1 E1 Framer control*



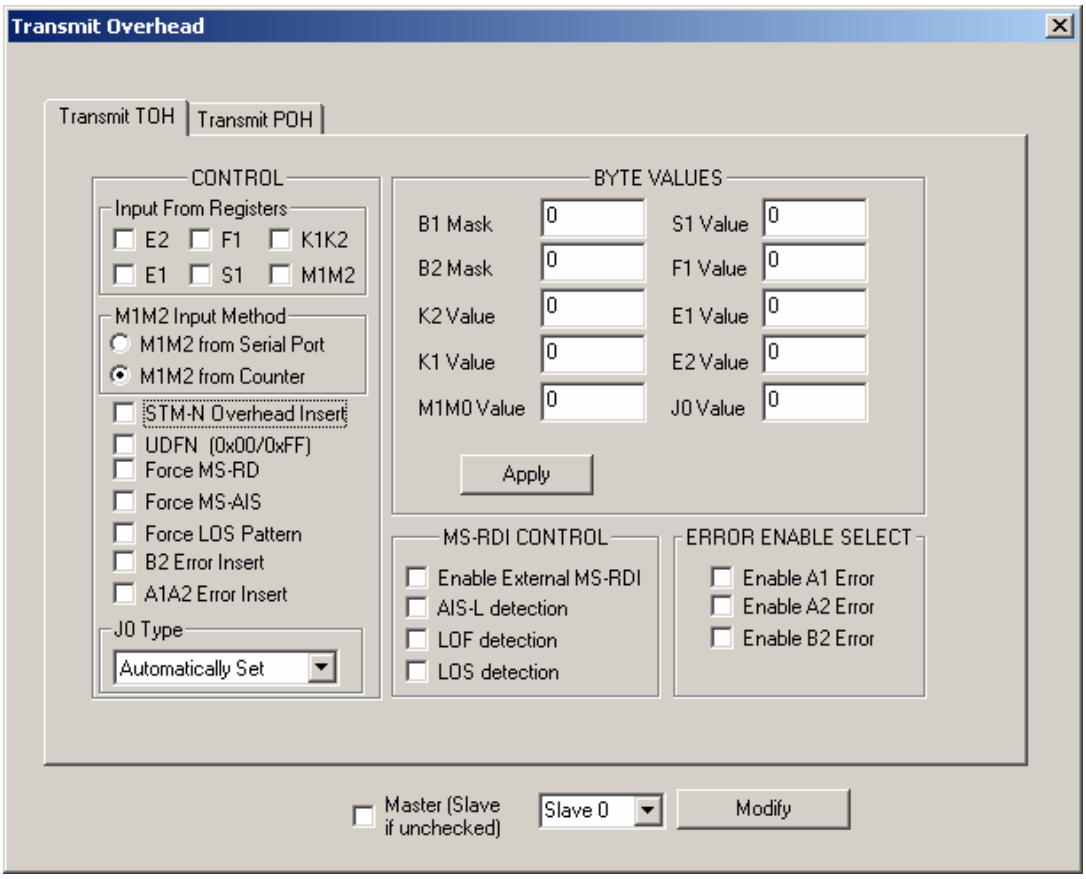
#### 4.3.5.2 E1 Interrupt Enable



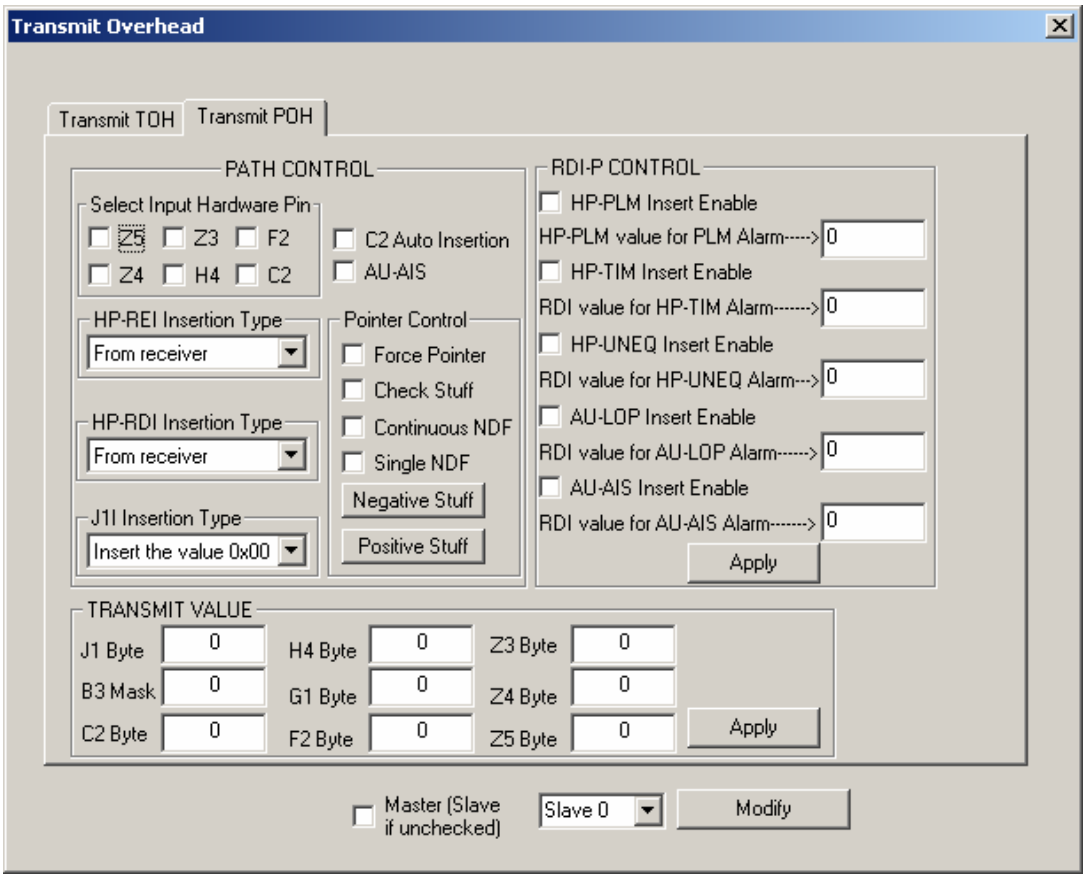
### 4.3.6 Transmit SDH Overhead

The following shows the two pages on the Transmit Overhead dialog

#### *4.3.6.1 Transmit Regenerator and Multiplex Section Overhead*



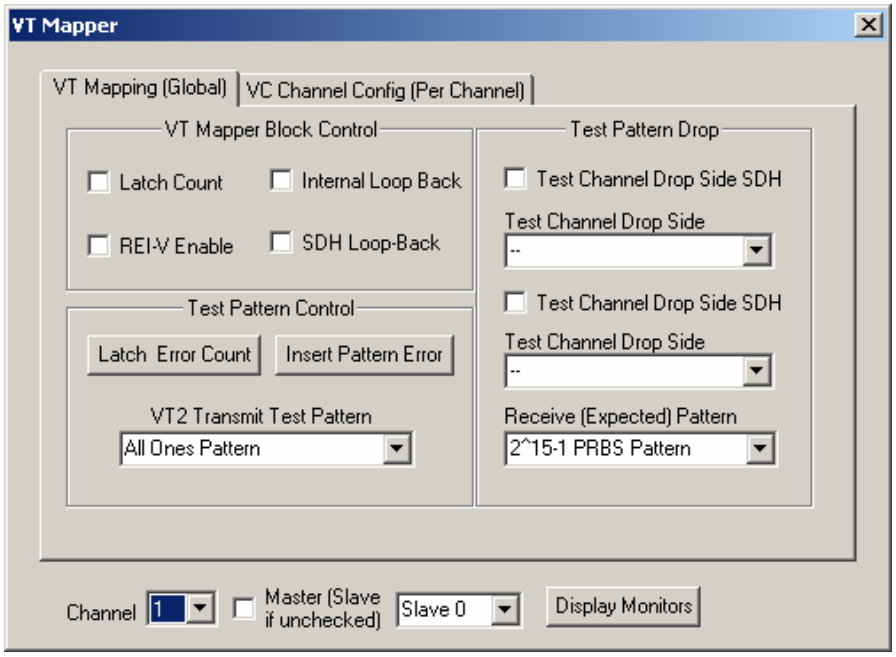
#### 4.3.6.2 Transmit High-Order Path Overhead



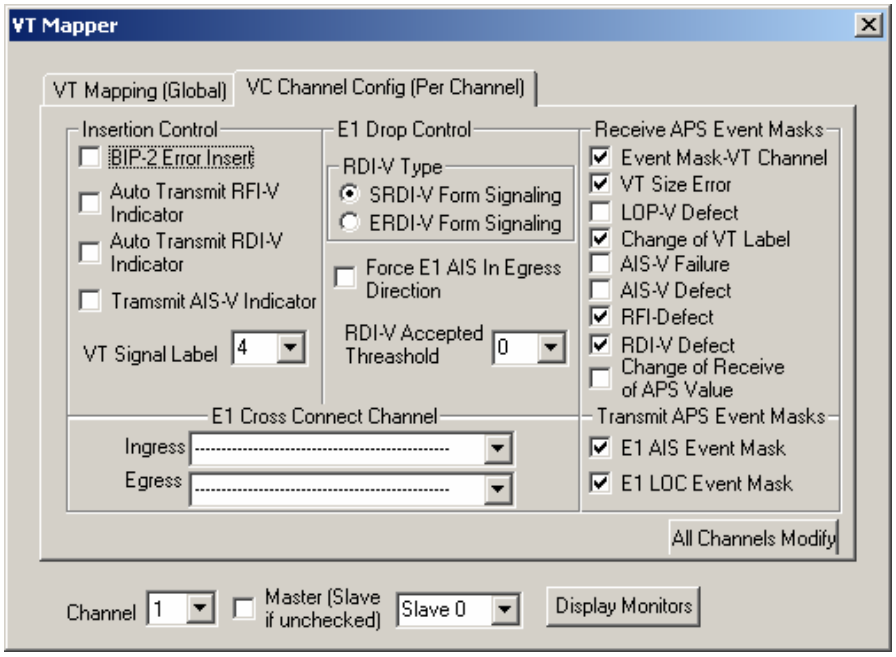
### 4.3.7 VT Mapper

The following are the two pages in VT Mapper block control. Click Display Monitors to display status indicators.

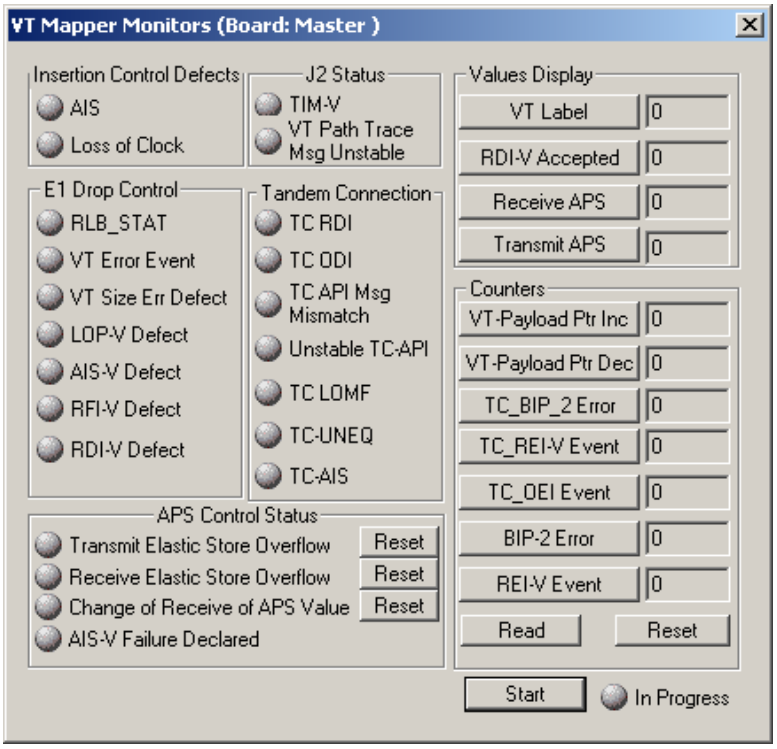
#### *4.3.7.1 Global VT Mapper Control*




#### *4.3.7.2 Channelized VT Mapper Control*

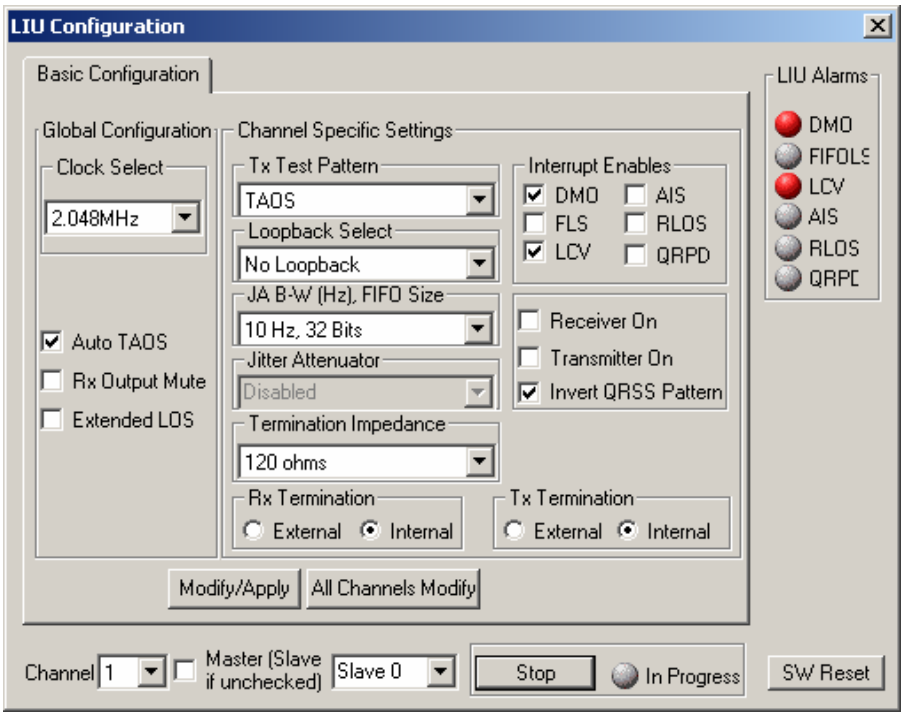


#### *4.3.7.3 VT Mapper Performance Monitors*



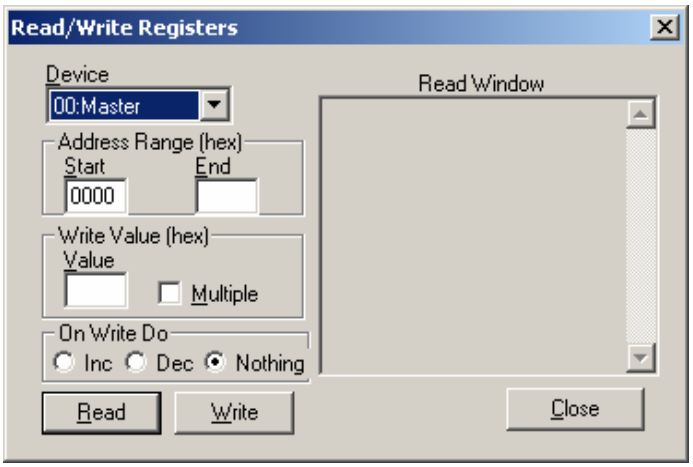

### 4.3.8 E1 Line Inferface Unit Configuration and Control

Use this dialog to control the LIU block. Indictors on the right show alarm signals.



### 4.3.9 Register Read/Write Access

Use this dialog to access, read or write, values in specified registers.



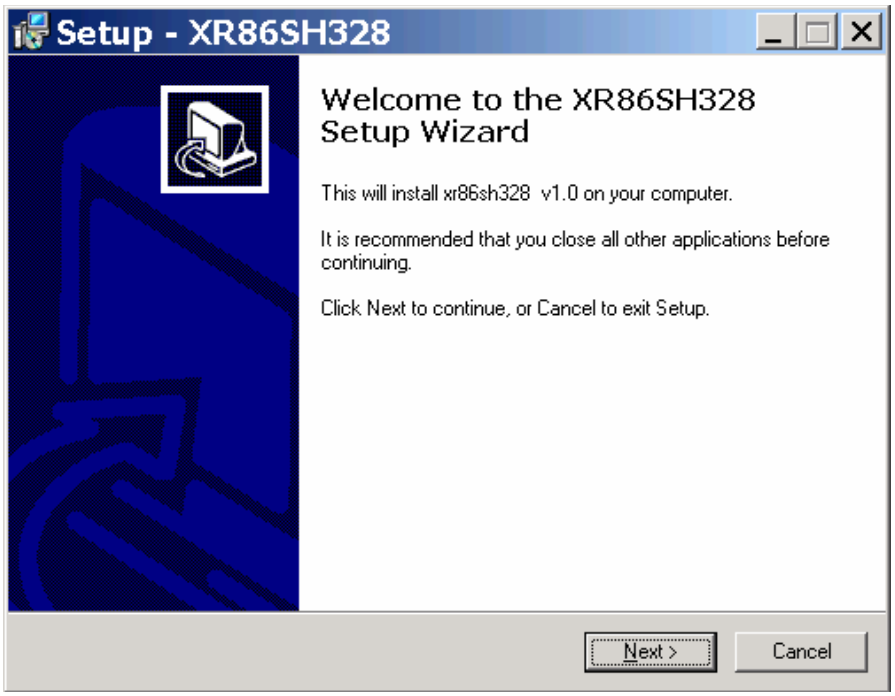
## 5.0 THE XRT86SH328 TRIPLE VOYAGER GRAPHICAL USER INTERFACE

The GUI is intended to allow easy access to configure basic registers in the 3 Voyager devices on the reference design platform.

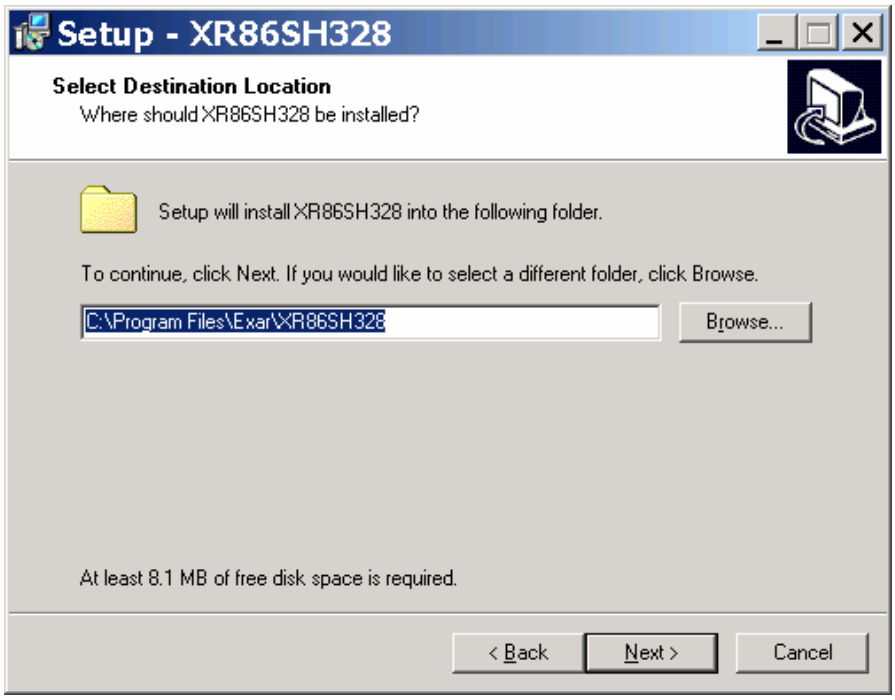
### *5.1 XRT86SH328 Triple Voyager GUI Setup and Installation*

Included in every Orion Modular Reference Design Platform is an Installation file. Located within the contents of the CDROM, the installation filename for the XRT86SH328 Triple Voyager Reference Design Platform is called "***XR86SH328 setup.exe***". This file will automatically load the Exar USB drivers and install the XRT86SH328 Triple Voyager Reference Design Platform GUI software. However, if the following steps are performed and the board is NOT recognized by the PC, **SEE"MANUALLY LOADING EXAR DRIVERS (IF INSTALLATION IS NOT SUCCESSFUL)" ON PAGE 37.** that describes how to manually load the drivers.

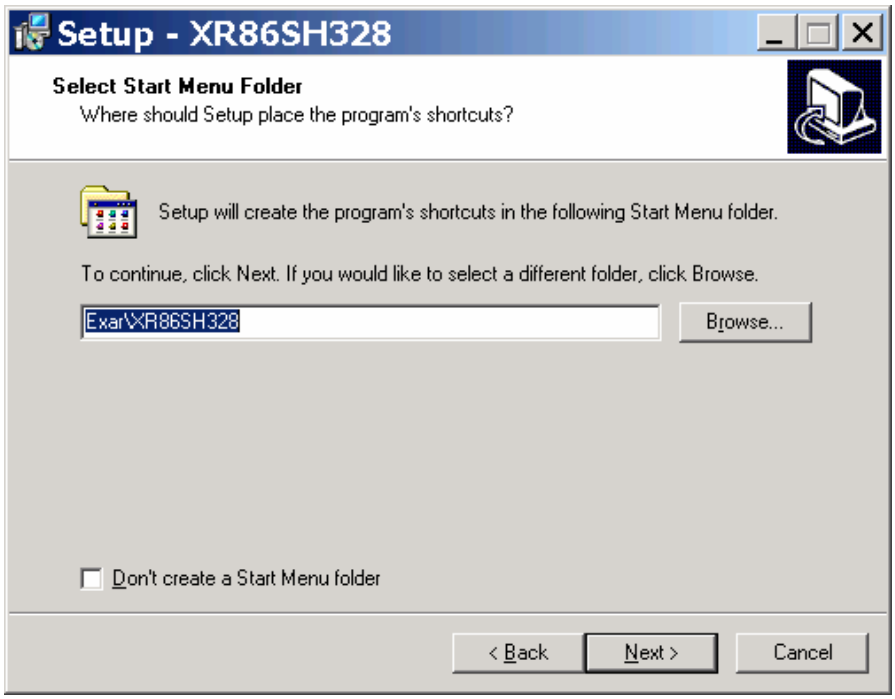
**Step 1** Double Click the "***XR86SH328 setup.exe***" file to bring up the following screen. Click on the **Next>** button.



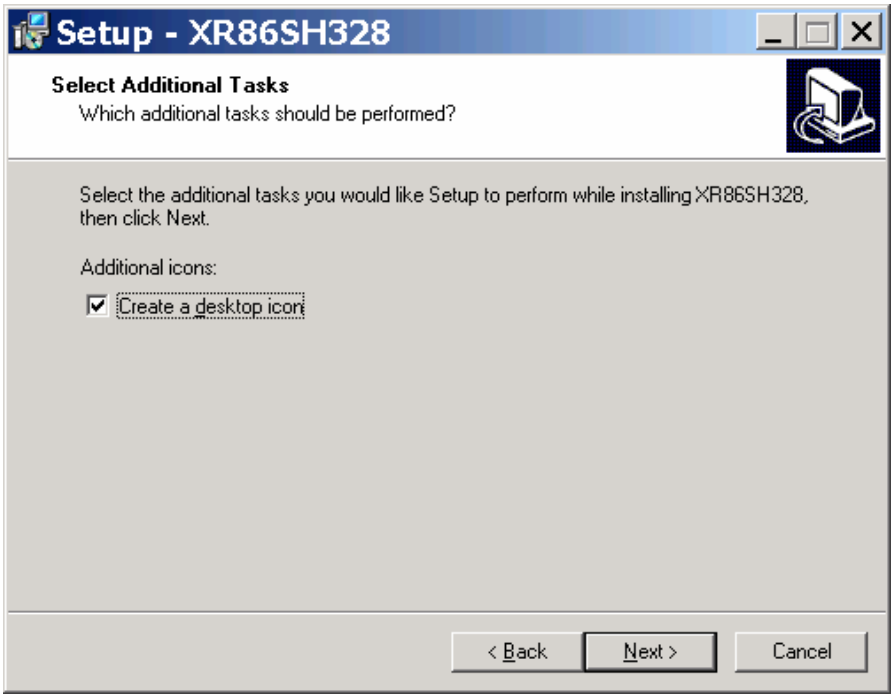
**Step 2** If there are no changes to the installation directory, Click on the **Next>** button to proceed. Otherwise, make the necessary changes and Click on the **Next>** button to proceed.



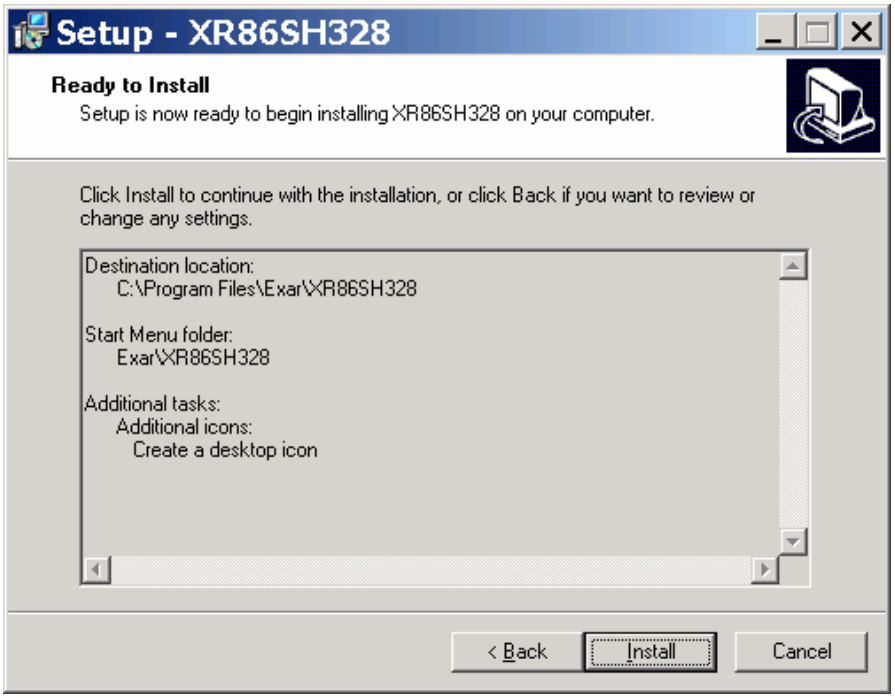

**Step 3** Click the **Next>** button to continue.



**Step 4** Select or De-select **Create a Deskstop Icon**. Click the **Next>** button to continue.




**Step 5** Click on the **Install** button to continue installation.

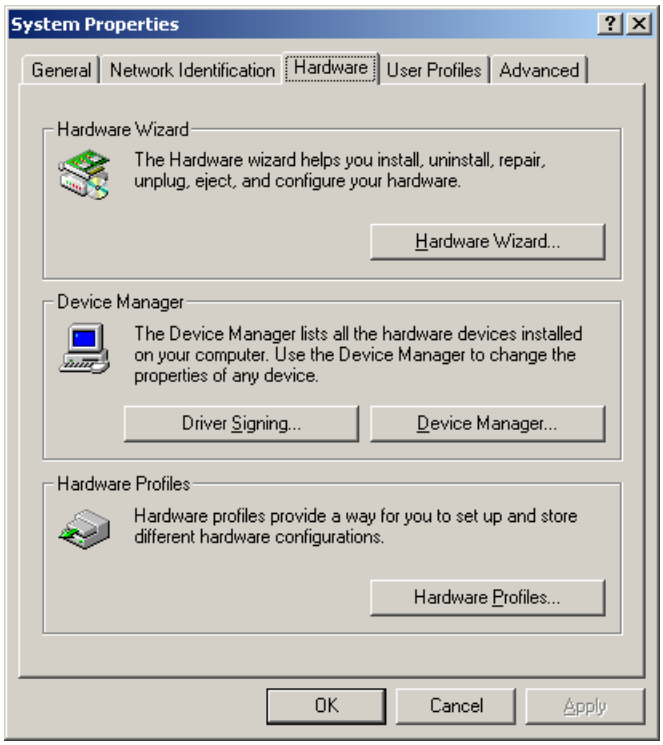


**Step 6** Click on the **Finish** button to complete installation. The Exar USB drivers should be properly installed and ready to go. If so, continue to the next section that describes the Graphical User Interface. If not, see **SEE"MANUALLY LOADING EXAR DRIVERS (IF INSTALLATION IS NOT SUCCESSFUL)" ON PAGE 37.** to manually load the Exar USB Drivers.

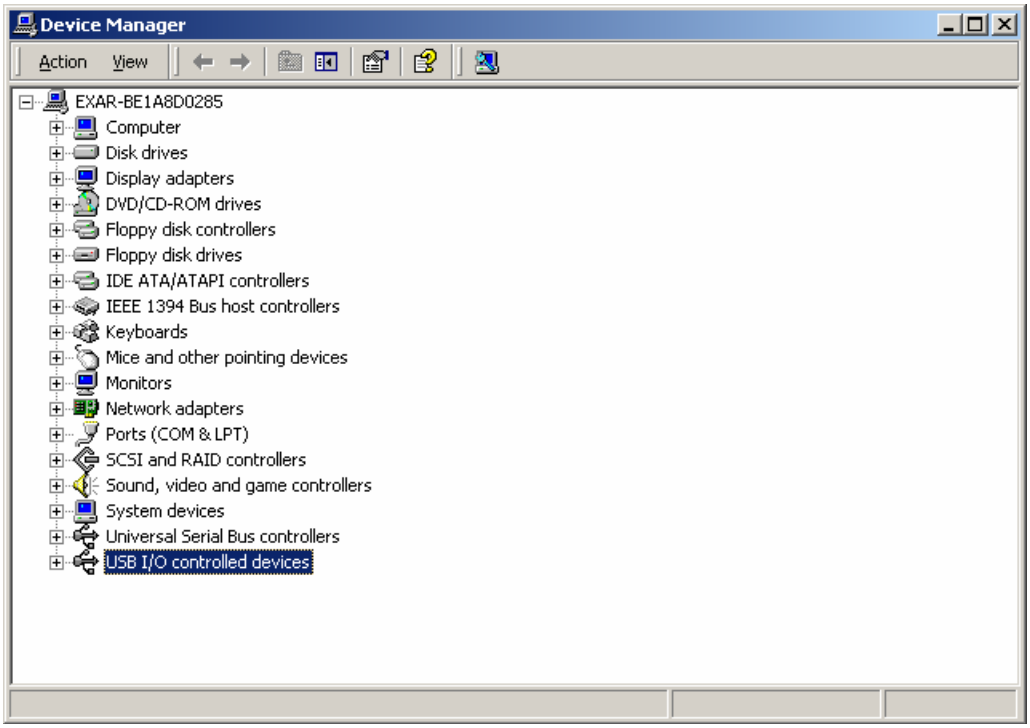
### 5.1.1 Manually Loading Exar Drivers (If Installation is NOT Successful)

If the Evaluation Board is NOT recognized and/or the installation process was NOT successful, most likely there is a driver contention or the driver was not installed in the proper directory from the software. This section describes how to manually load the drivers.

Note: Each Windows operating system may access the System Hardware differently. Therefore, it is not practical to describe this procedure for each OS. However, the key component is usually the Control Panel of the PC. From the Control Panel, you can access the System Properties dialog box. From there, choose the Hardware menu item and go to the Device Manager…



The device Manager will bring up the following dialog box. Choose the USB I/O Controlled Devices, select Exar Device, right click, select properties, select Update Driver, and then follow the directions to choose the driver from the CD or the /Driver directory in the Exar working directory ("C:\Program Files\Exar\3VoyagerLites Evaluation Software" by default).



## 6.0 STARTING THE XRT86SH328 TRIPLE VOYAGER GUI

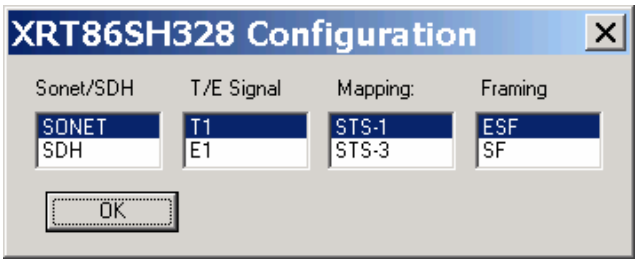
The evaluation software allows the user to do the following:

- Configure the XRT86SH328 for proper operation
- Poll current and historical performance status
- Download the FPGA code
- Enable/Disable XRT86SH328 features with the click of a button

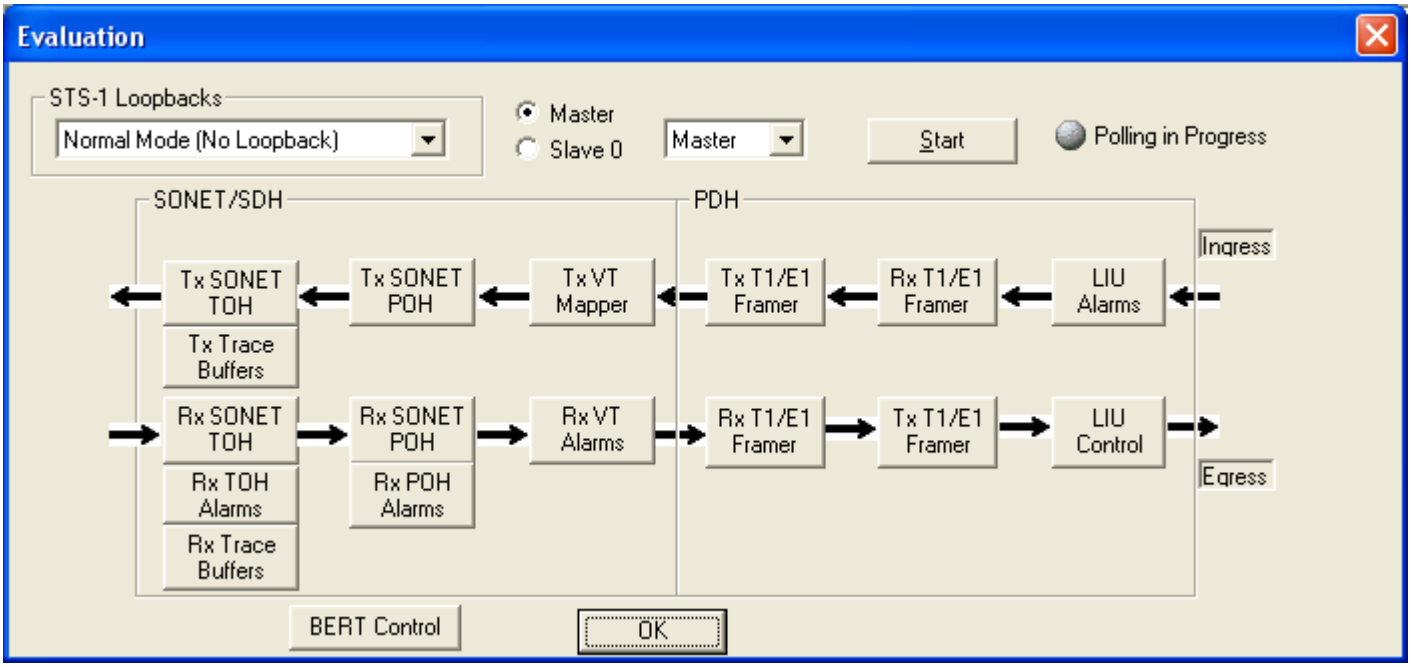
After launching the executable, select the option corresponding to the hardware evaluation system you have.


FPGA download was successful.

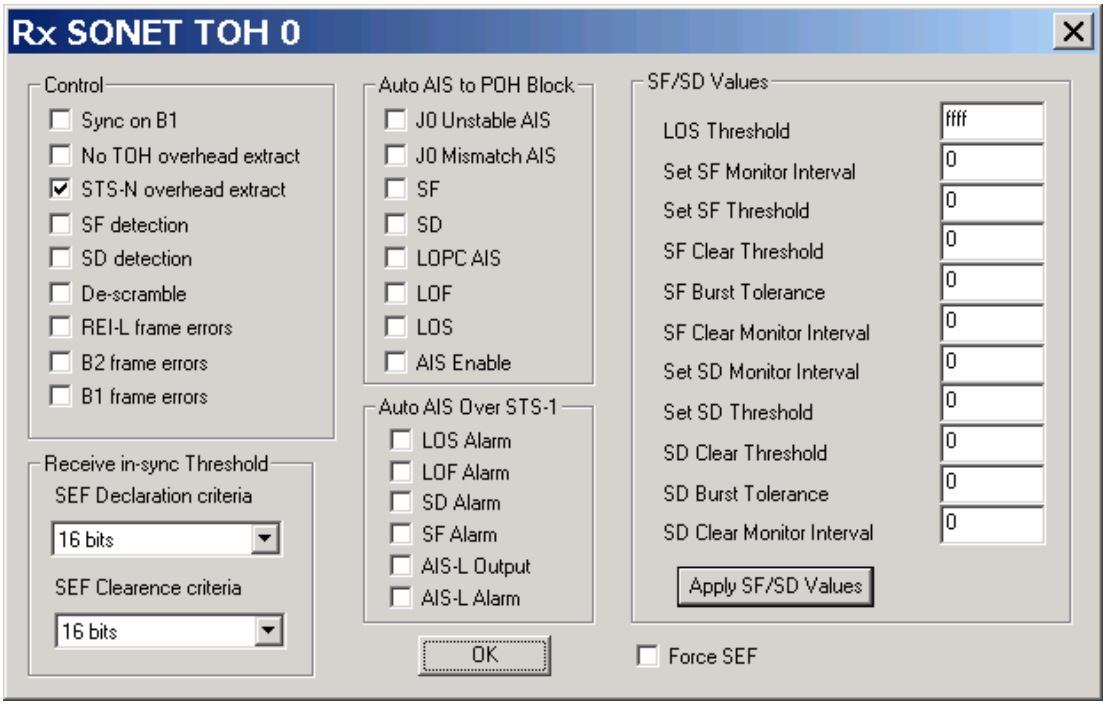
Select the fields that the application will use and the board can support.



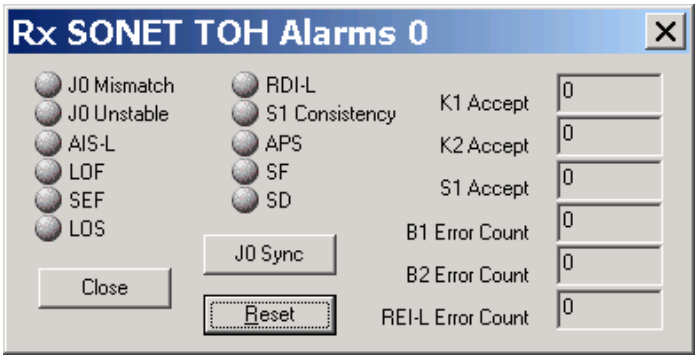

### 6.0.1 Main Evaluation Menu.



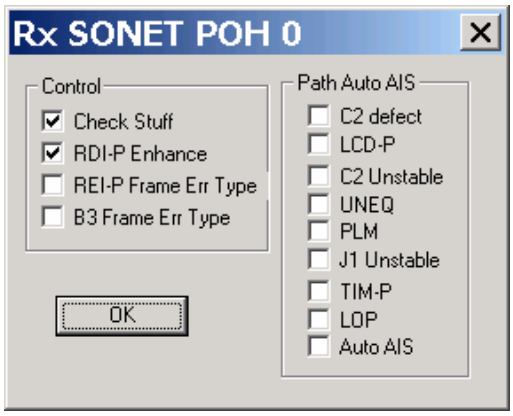
### 6.0.2 Receive SONET Transport Overhead /SDH Regenerator and Multiplex Section Configuration



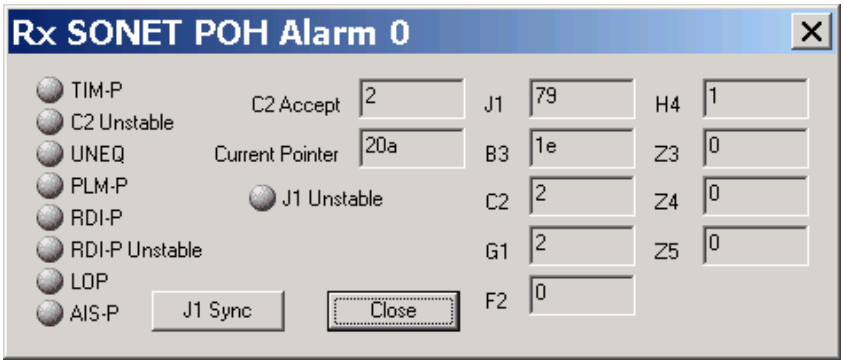

#### *6.0.2.1 Receive SONET Transport Overhead /SDH Regenerator and Multiplex Section Performance Monitoring Alarms*



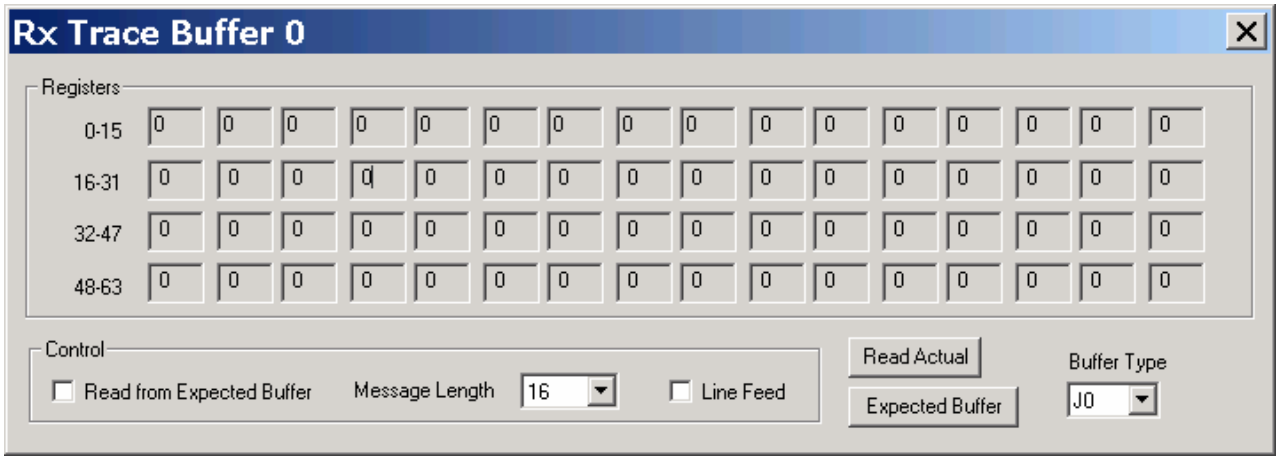
### 6.0.3 Receive SONET Path Overhead /SDH High-Order Path Configuration



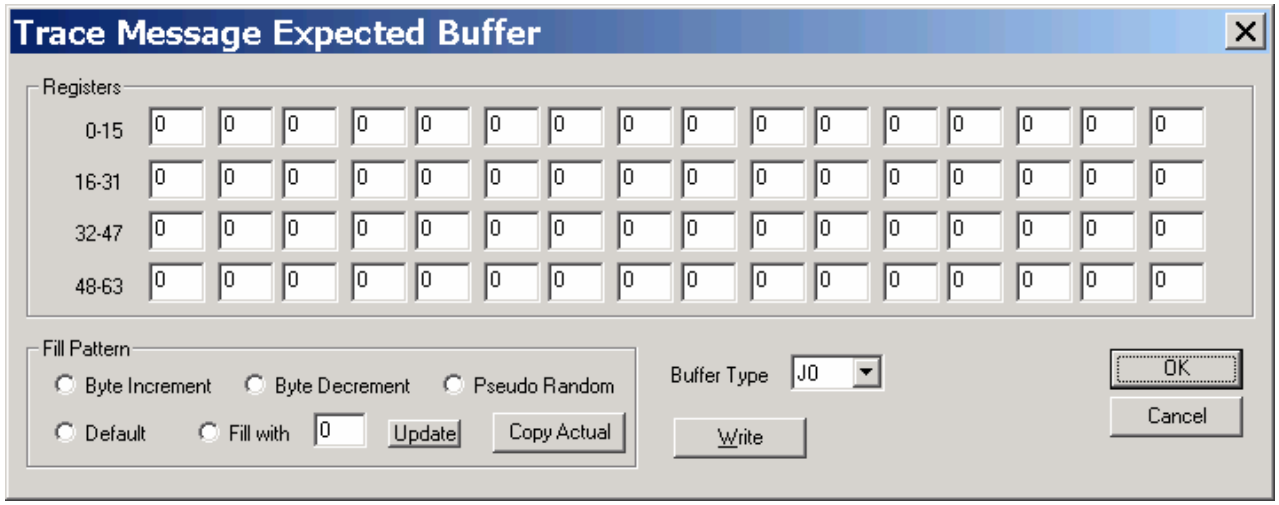

#### *6.0.3.1 Receive SONET Path Overhead /SDH High-Order Path Performance Monitoring Alarms*



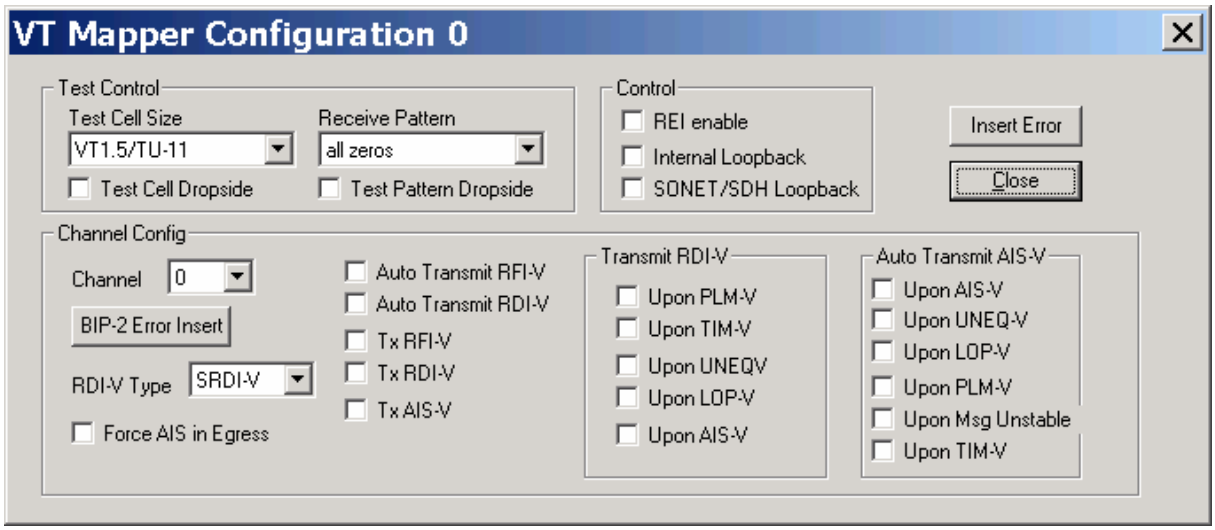
### 6.0.4 Receive Validated SONET (J0) Section and (J1) Path and (J2) VT-Path Trace Buffer /SDH (J0) Regenerator Section and (J1) High-Order Path and (J2) Low-Order Path Trace Message Buffer



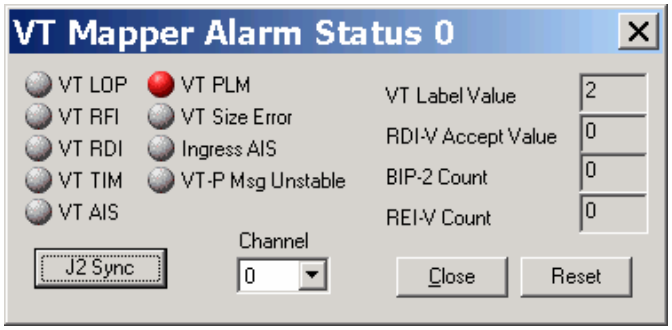

### 6.0.5 Receive Expected SONET (J0) Section and (J1) Path and (J2) VT-Path Trace Buffer /SDH (J0) Regenerator Section and (J1) High-Order Path and (J2) Low-Order Path Trace Message Buffer



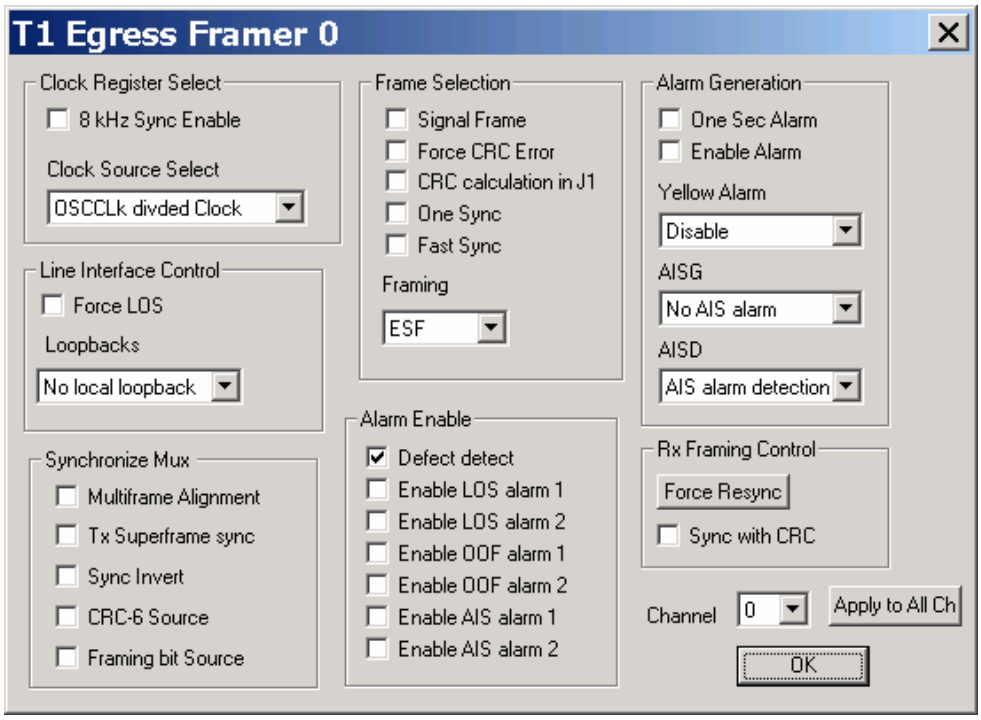
### 6.0.6 VT Mapper Configuration



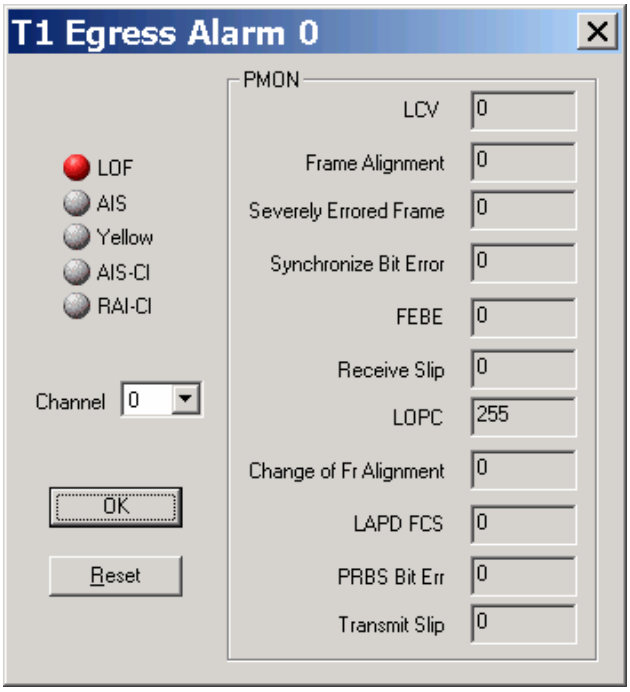

#### *6.0.6.1 VT Mapper Alarms*



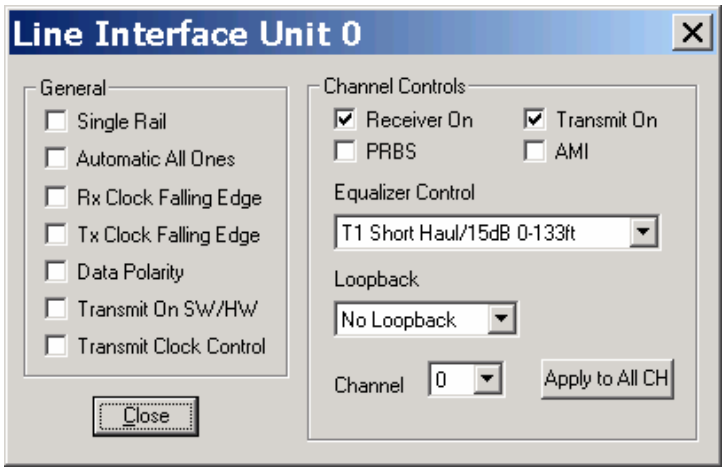
### 6.0.7 T1 Egress Configuration




#### *6.0.7.1 T1 Egress Alarms*

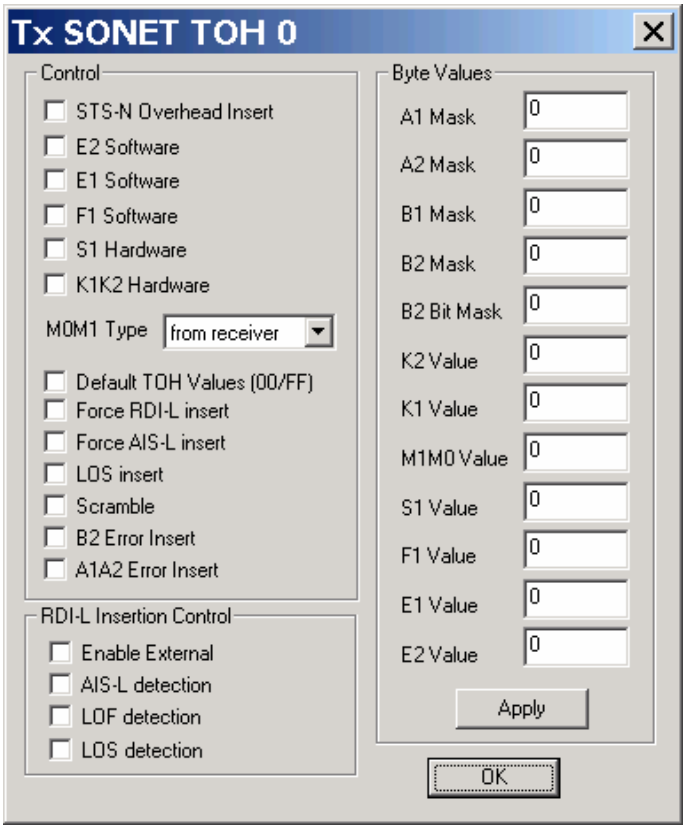


### 6.0.8 Line Interface Unit Configuration

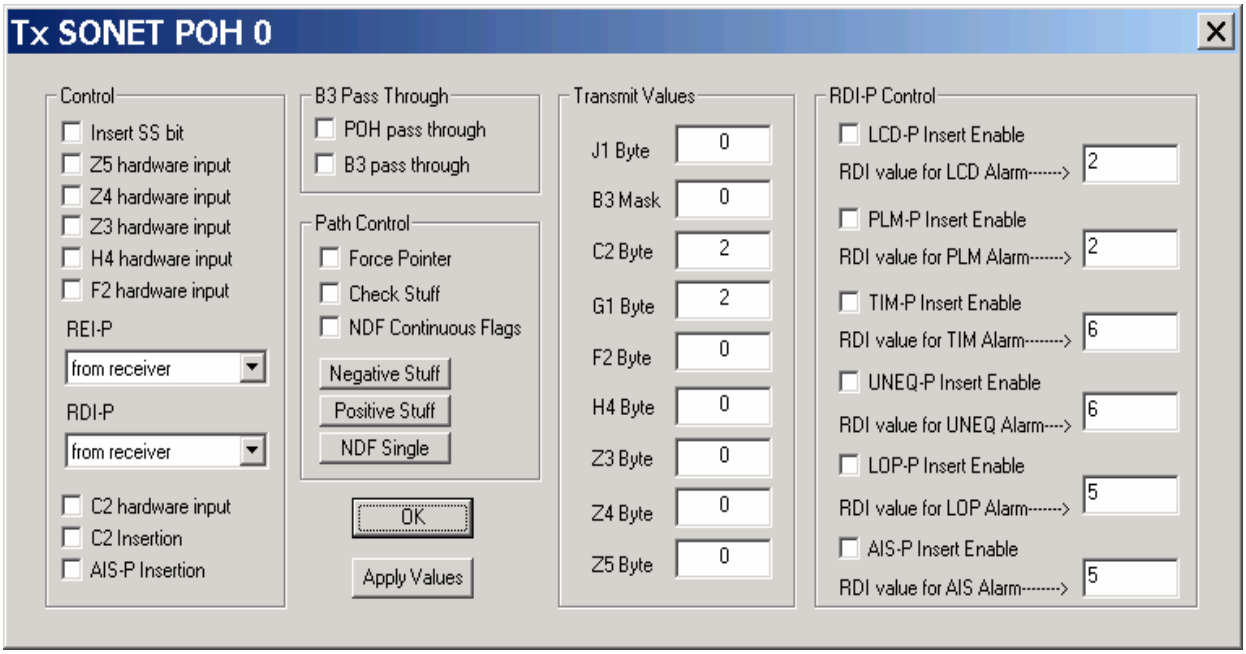



#### *6.0.8.1 Line Interface Unit Performance Monitoring Alarms*

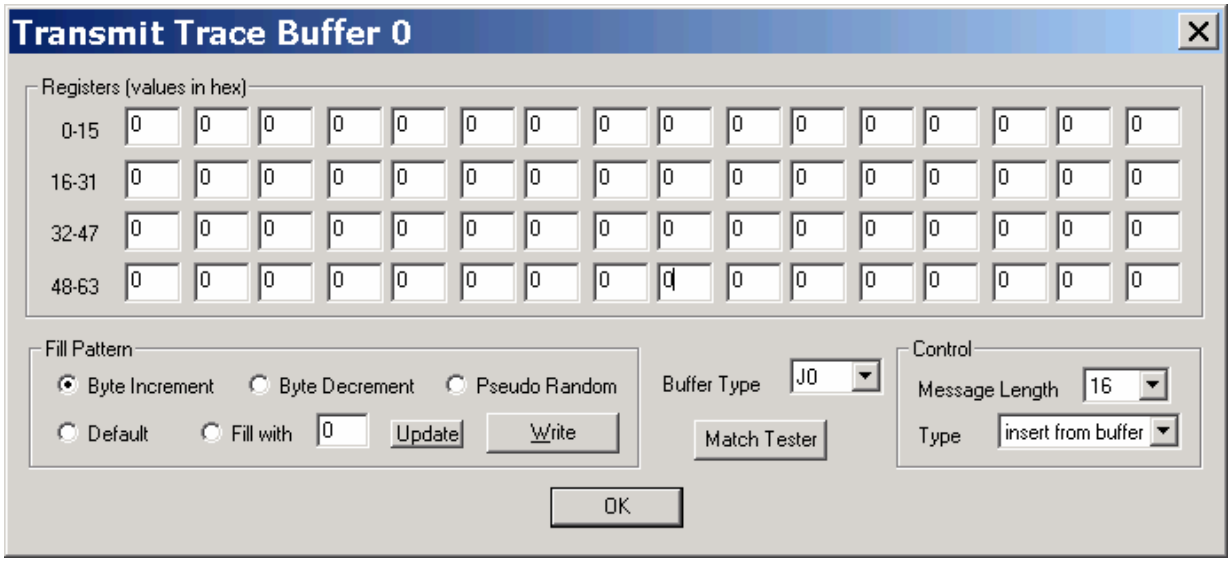
### 6.0.9 Transmit SONET Transport Overhead Configuration



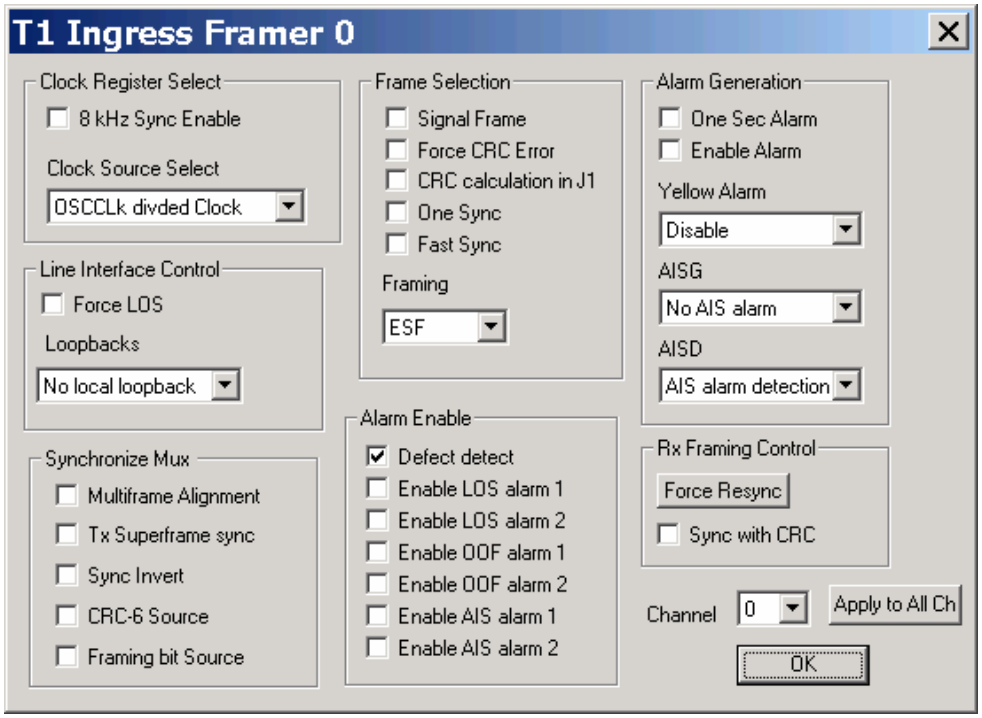

### 6.0.10 Transmit SONET Path Overhead Configuration



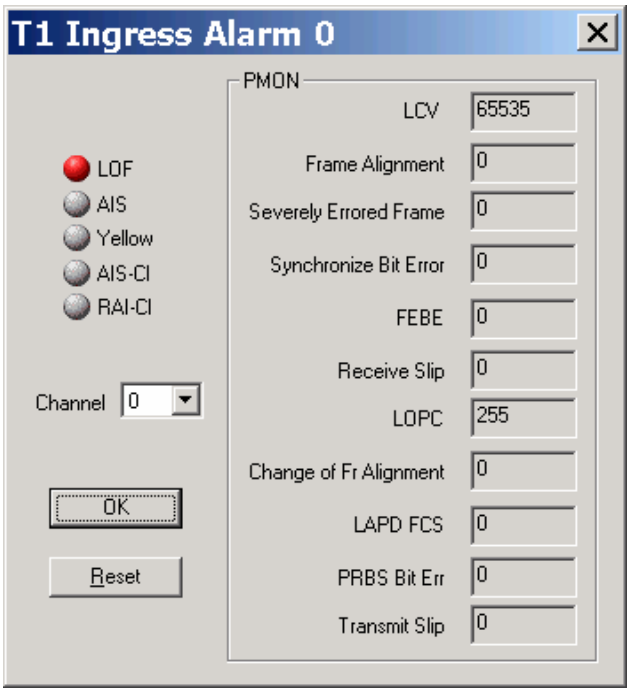
### 6.0.11 Transmit *SONET (J0) Section and (J1) Path and (J2) VT-Path Trace Buffer /SDH (J0) Regenerator Section and (J1) High-Order Path and (J2) Low-Order Path Trace Message Buffer*




### 6.0.12 T1 Ingress Configuration



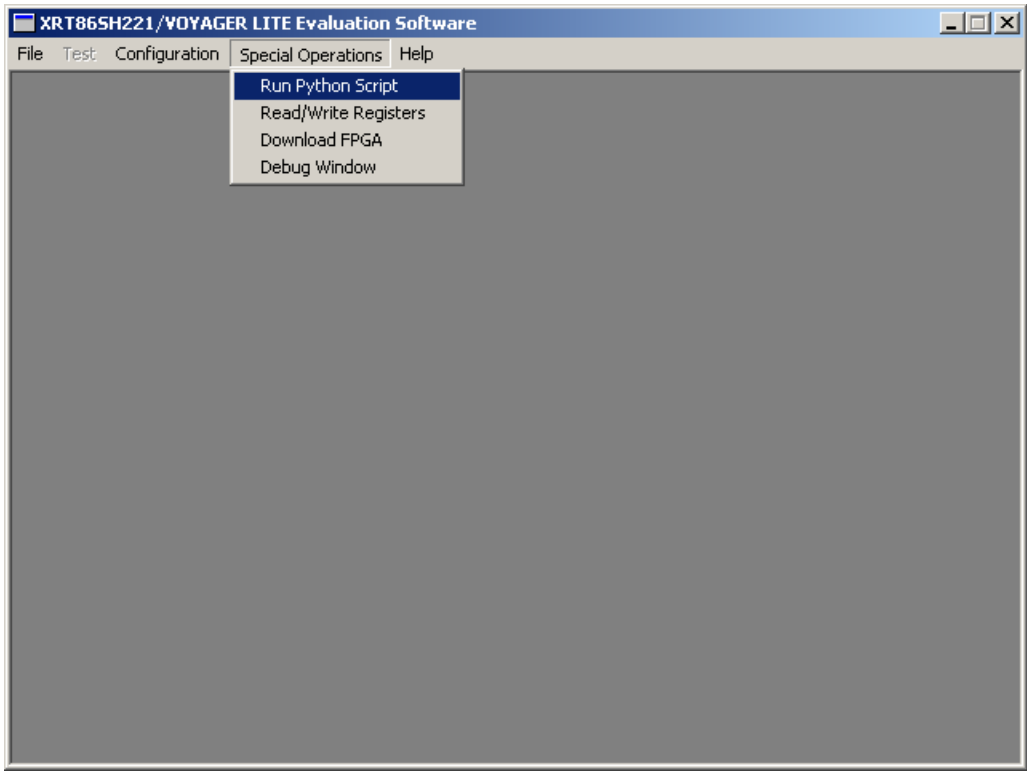
#### *6.0.12.1 T1 Ingress Alarms*



## 7.0 PYTHON SCRIPT INTERFACE

### Running a Python Script From the GUI

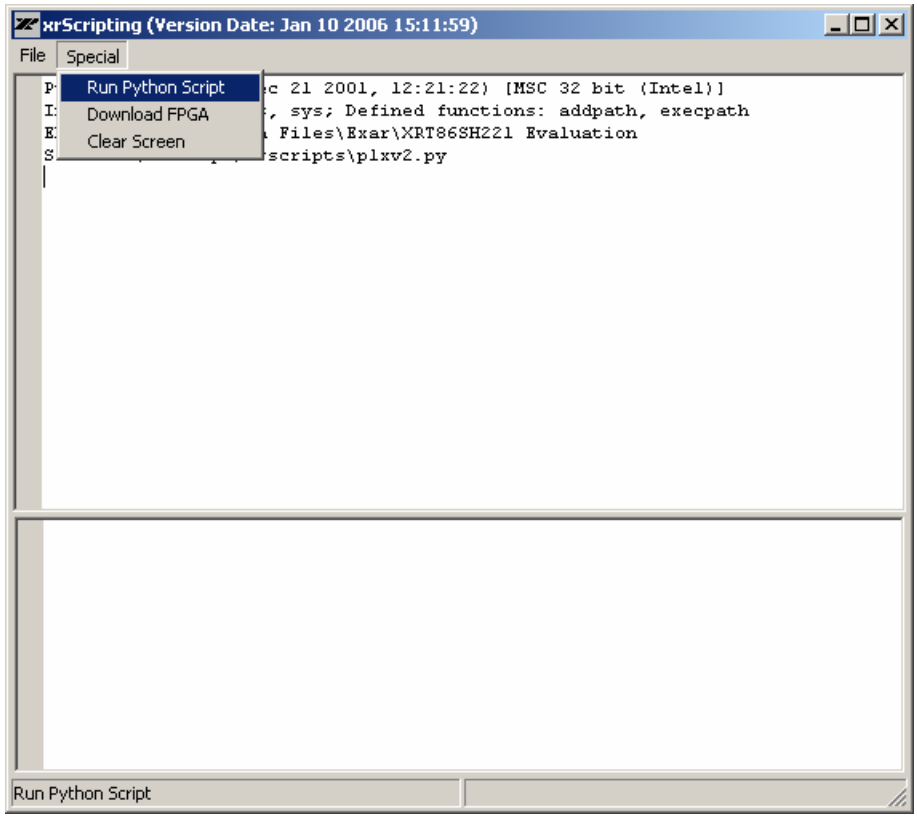
From the main GUI, select the Special Operations menu shown below and click on the "Run Python Script" to continue.



Once you select the "Run Python Script" option from the Special Operations menu from the GUI, the "xrScripting Interface" will pop-up as shown below. At this point, the xrScripting Interface is independent of the GUI and any script files that are run will automatically overwrite the GUI settings if there is an overlap with the registers. Therefore, caution must be used to keep track of the register configurations if one wants to toggle back and forth from the

GUI to the xrScripting Interface. The next step is to use the "Special" menu on the tool bar to run the actual test script file.

Note: If you would like to view a particular test script in a plain text editor mode, use the "File" menu on the tool bar and select "Open".



## 8.0 XRT86SH221 E1 TEST HEADERS H3 AND H4

There are two test headers H3 and H4 on Front Panel of the XRT86SH221 Triple Voyager Lite device platform. These permit access to all 63 possible E1 channels. Below is a magnified view of the XRT86SH221 Triple Voyager test header diagram. The following table has the complete tip and ring transmission and reception lines in reference to channel assigment location on the H3 and H4 test headers.

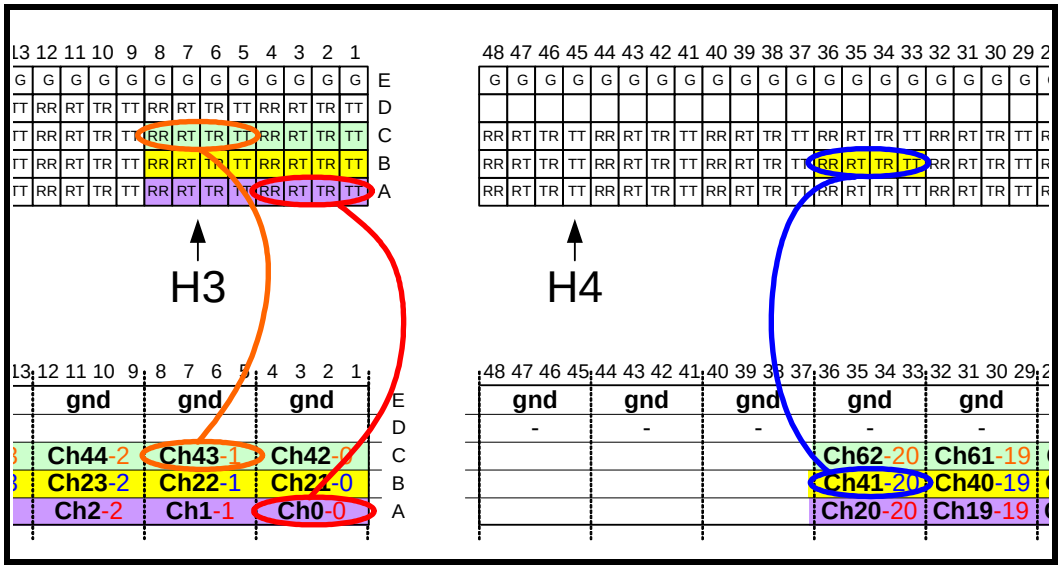



**TABLE 1: TRIPLE VOYAGER LITE CHANNEL TO PIN LOCATION CROSS REFERENCE GUIDE**

| E1 CHANNEL | XRT86SH221 | DEVICE CHANNEL | HEADER | PIN LOCATION | | | |
|---|---|---|---|---|---|---|---|
| | | | | TTIP | TRING | RTIP | RRING |
| **0** | U2 - Master | 0 | H3 | A1 | A2 | A3 | A4 |
| **1** | U2 - Master | 1 | H3 | A5 | A6 | A7 | A8 |
| **2** | U2 - Master | 2 | H3 | A9 | A10 | A11 | A12 |
| **3** | U2 - Master | 3 | H3 | A13 | A14 | A15 | A16 |
| **4** | U2 - Master | 4 | H3 | A17 | A18 | A19 | A20 |
| **5** | U2 - Master | 5 | H3 | A21 | A22 | A23 | A24 |
| **6** | U2 - Master | 6 | H3 | A25 | A26 | A27 | A28 |
| **7** | U2 - Master | 7 | H3 | A29 | A30 | A31 | A32 |
| **8** | U2 - Master | 8 | H3 | A33 | A34 | A35 | A36 |
| **9** | U2 - Master | 9 | H3 | A37 | A38 | A39 | A40 |

TABLE 1: TRIPLE VOYAGER LITE CHANNEL TO PIN LOCATION CROSS REFERENCE GUIDE

| E1 CHANNEL | XRT86SH221 | DEVICE CHANNEL | HEADER | PIN LOCATION | | | |
|---|---|---|---|---|---|---|---|
| | | | | TTIP | TRING | RTIP | RRING |
| **10** | U2 - Master | 10 | H3 | A41 | A42 | A43 | A44 |
| **11** | U2 - Master | 11 | H3 | A45 | A46 | A47 | A48 |
| **12** | U2 - Master | 12 | H4 | A1 | A2 | A3 | A4 |
| **13** | U2 - Master | 13 | H4 | A5 | A6 | A7 | A8 |
| **14** | U2 - Master | 14 | H4 | A9 | A10 | A11 | A12 |
| **15** | U2 - Master | 15 | H4 | A13 | A14 | A15 | A16 |
| **16** | U2 - Master | 16 | H4 | A17 | A18 | A19 | A20 |
| **17** | U2 - Master | 17 | H4 | A21 | A22 | A23 | A24 |
| **18** | U2 - Master | 18 | H4 | A25 | A26 | A27 | A28 |
| **19** | U2 - Master | 19 | H4 | A29 | A30 | A31 | A32 |
| **20** | U2 - Master | 20 | H4 | A33 | A34 | A35 | A36 |
| **21** | U3 - Slave 1 | 0 | H3 | B1 | B2 | B3 | B4 |
| **22** | U3 - Slave 1 | 1 | H3 | B5 | B6 | B7 | B8 |
| **23** | U3 - Slave 1 | 2 | H3 | B9 | B10 | B11 | B12 |
| **24** | U3 - Slave 1 | 3 | H3 | B13 | B14 | B15 | B16 |
| **25** | U3 - Slave 1 | 4 | H3 | B17 | B18 | B19 | B20 |
| **26** | U3 - Slave 1 | 5 | H3 | B21 | B22 | B23 | B24 |
| **27** | U3 - Slave 1 | 6 | H3 | B25 | B26 | B27 | B28 |
| **28** | U3 - Slave 1 | 7 | H3 | B29 | B30 | B31 | B32 |
| **29** | U3 - Slave 1 | 8 | H3 | B33 | B34 | B35 | B36 |
| **30** | U3 - Slave 1 | 9 | H3 | B37 | B38 | B39 | B40 |
| **31** | U3 - Slave 1 | 10 | H3 | B41 | B42 | B43 | B44 |
| **32** | U3 - Slave 1 | 11 | H3 | B45 | B46 | B47 | B48 |
| **33** | U3 - Slave 1 | 12 | H4 | B1 | B2 | B3 | B4 |
| **34** | U3 - Slave 1 | 13 | H4 | B5 | B6 | B7 | B8 |
| **35** | U3 - Slave 1 | 14 | H4 | B9 | B10 | B11 | B12 |
| **36** | U3 - Slave 1 | 15 | H4 | B13 | B14 | B15 | B16 |
| **37** | U3 - Slave 1 | 16 | H4 | B17 | B18 | B19 | B20 |
| **38** | U3 - Slave 1 | 17 | H4 | B21 | B22 | B23 | B24 |
| **39** | U3 - Slave 1 | 18 | H4 | B25 | B26 | B27 | B28 |
| **40** | U3 - Slave 1 | 19 | H4 | B29 | B30 | B31 | B32 |

TABLE 1: TRIPLE VOYAGER LITE CHANNEL TO PIN LOCATION CROSS REFERENCE GUIDE

| E1 CHANNEL | XRT86SH221 | DEVICE CHANNEL | HEADER | PIN LOCATION | | | |
|---|---|---|---|---|---|---|---|
| | | | | TTIP | TRING | RTIP | RRING |
| **41** | U3 - Slave 1 | 20 | H4 | B33 | B34 | B35 | B36 |
| **42** | U4 - Slave 2 | 0 | H3 | C1 | C2 | C3 | C4 |
| **43** | U4 - Slave 2 | 1 | H3 | C5 | C6 | C7 | C8 |
| **44** | U4 - Slave 2 | 2 | H3 | C9 | C10 | C11 | C12 |
| **45** | U4 - Slave 2 | 3 | H3 | C13 | C14 | C15 | C16 |
| **46** | U4 - Slave 2 | 4 | H3 | C17 | C18 | C19 | C20 |
| **47** | U4 - Slave 2 | 5 | H3 | C21 | C22 | C23 | C24 |
| **48** | U4 - Slave 2 | 6 | H3 | C25 | C26 | C27 | C28 |
| **49** | U4 - Slave 2 | 7 | H3 | C29 | C30 | C31 | C32 |
| **50** | U4 - Slave 2 | 8 | H3 | C33 | C34 | C35 | C36 |
| **51** | U4 - Slave 2 | 9 | H3 | C37 | C38 | C39 | C40 |
| **52** | U4 - Slave 2 | 10 | H3 | C41 | C42 | C43 | C44 |
| **53** | U4 - Slave 2 | 11 | H3 | C45 | C46 | C47 | C48 |
| **54** | U4 - Slave 2 | 12 | H4 | C1 | C2 | C3 | C4 |
| **55** | U4 - Slave 2 | 13 | H4 | C5 | C6 | C7 | C8 |
| **56** | U4 - Slave 2 | 14 | H4 | C9 | C10 | C11 | C12 |
| **57** | U4 - Slave 2 | 15 | H4 | C13 | C14 | C15 | C16 |
| **58** | U4 - Slave 2 | 16 | H4 | C17 | C18 | C19 | C20 |
| **59** | U4 - Slave 2 | 17 | H4 | C21 | C22 | C23 | C24 |
| **60** | U4 - Slave 2 | 18 | H4 | C25 | C26 | C27 | C28 |
| **61** | U4 - Slave 2 | 19 | H4 | C29 | C30 | C31 | C32 |
| **62** | U4 - Slave 2 | 20 | H4 | C33 | C34 | C35 | C36 |

## 9.0 XRT86SH328 T1/J1 TEST HEADERS H3 AND H4

There are two test headers H3 and H4 on Front Panel of the XRT86SH328 Triple Voyager device platform. These permit access to all 84 possible T1 or J1 channels. Below is a magnified view of the XRT86SH328 Triple Voyager test header diagram. The following table has the complete tip and ring transmission and reception lines in reference to channel assigment location on the H3 and H4 test headers.

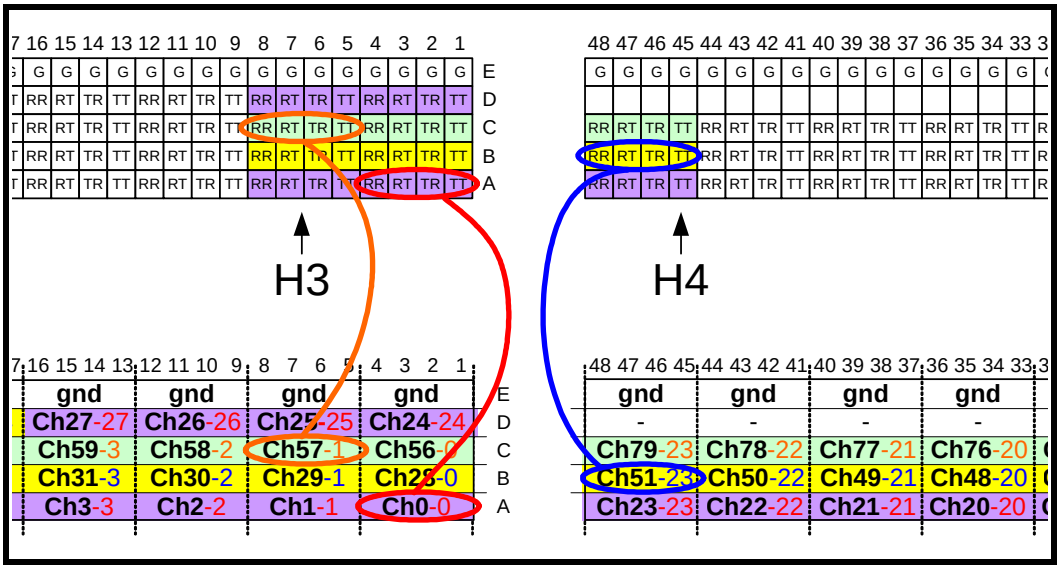



**TABLE 2: TRIPLE VOYAGER CHANNEL TO PIN LOCATION CROSS REFERENCE GUIDE**

| T1/J1 CHANNEL | XRT86SH328 | DEVICE CHANNEL | HEADER | PIN LOCATION | | | |
|---|---|---|---|---|---|---|---|
| | | | | TTIP | TRING | RTIP | RRING |
| **0** | U2 - Master | 0 | H3 | A1 | A2 | A3 | A4 |
| **1** | U2 - Master | 1 | H3 | A5 | A6 | A7 | A8 |
| **2** | U2 - Master | 2 | H3 | A9 | A10 | A11 | A12 |
| **3** | U2 - Master | 3 | H3 | A13 | A14 | A15 | A16 |
| **4** | U2 - Master | 4 | H3 | A17 | A18 | A19 | A20 |
| **5** | U2 - Master | 5 | H3 | A21 | A22 | A23 | A24 |
| **6** | U2 - Master | 6 | H3 | A25 | A26 | A27 | A28 |
| **7** | U2 - Master | 7 | H3 | A29 | A30 | A31 | A32 |
| **8** | U2 - Master | 8 | H3 | A33 | A34 | A35 | A36 |
| **9** | U2 - Master | 9 | H3 | A37 | A38 | A39 | A40 |

TABLE 2: TRIPLE VOYAGER CHANNEL TO PIN LOCATION CROSS REFERENCE GUIDE

| T1/J1 CHANNEL | XRT86SH328 | DEVICE CHANNEL | HEADER | PIN LOCATION | | | |
|---|---|---|---|---|---|---|---|
| | | | | TTIP | TRING | RTIP | RRING |
| **10** | U2 - Master | 10 | H3 | A41 | A42 | A43 | A44 |
| **11** | U2 - Master | 11 | H3 | A45 | A46 | A47 | A48 |
| **12** | U2 - Master | 12 | H4 | A1 | A2 | A3 | A4 |
| **13** | U2 - Master | 13 | H4 | A5 | A6 | A7 | A8 |
| **14** | U2 - Master | 14 | H4 | A9 | A10 | A11 | A12 |
| **15** | U2 - Master | 15 | H4 | A13 | A14 | A15 | A16 |
| **16** | U2 - Master | 16 | H4 | A17 | A18 | A19 | A20 |
| **17** | U2 - Master | 17 | H4 | A21 | A22 | A23 | A24 |
| **18** | U2 - Master | 18 | H4 | A25 | A26 | A27 | A28 |
| **19** | U2 - Master | 19 | H4 | A29 | A30 | A31 | A32 |
| **20** | U2 - Master | 20 | H4 | A33 | A34 | A35 | A36 |
| **21** | U2 - Master | 21 | H4 | A37 | A38 | A39 | A40 |
| **22** | U2 - Master | 22 | H4 | A41 | A42 | A43 | A44 |
| **23** | U2 - Master | 23 | H4 | A45 | A46 | A47 | A48 |
| **24** | U2 - Master | 24 | H3 | D1 | D2 | D3 | D4 |
| **25** | U2 - Master | 25 | H3 | D5 | D6 | D7 | D8 |
| **26** | U2 - Master | 26 | H3 | D9 | D10 | D11 | D12 |
| **27** | U2 - Master | 27 | H3 | D13 | D14 | D15 | D16 |
| **28** | U3 - Slave 1 | 0 | H3 | B1 | B2 | B3 | B4 |
| **29** | U3 - Slave 1 | 1 | H3 | B5 | B6 | B7 | B8 |
| **30** | U3 - Slave 1 | 2 | H3 | B9 | B10 | B11 | B12 |
| **31** | U3 - Slave 1 | 3 | H3 | B13 | B14 | B15 | B16 |
| **32** | U3 - Slave 1 | 4 | H3 | B17 | B18 | B19 | B20 |
| **33** | U3 - Slave 1 | 5 | H3 | B21 | B22 | B23 | B24 |
| **34** | U3 - Slave 1 | 6 | H3 | B25 | B26 | B27 | B28 |
| **35** | U3 - Slave 1 | 7 | H3 | B29 | B30 | B31 | B32 |
| **36** | U3 - Slave 1 | 8 | H3 | B33 | B34 | B35 | B36 |
| **37** | U3 - Slave 1 | 9 | H3 | B37 | B38 | B39 | B40 |
| **38** | U3 - Slave 1 | 10 | H3 | B41 | B42 | B43 | B44 |
| **39** | U3 - Slave 1 | 11 | H3 | B45 | B46 | B47 | B48 |
| **40** | U3 - Slave 1 | 12 | H4 | B1 | B2 | B3 | B4 |

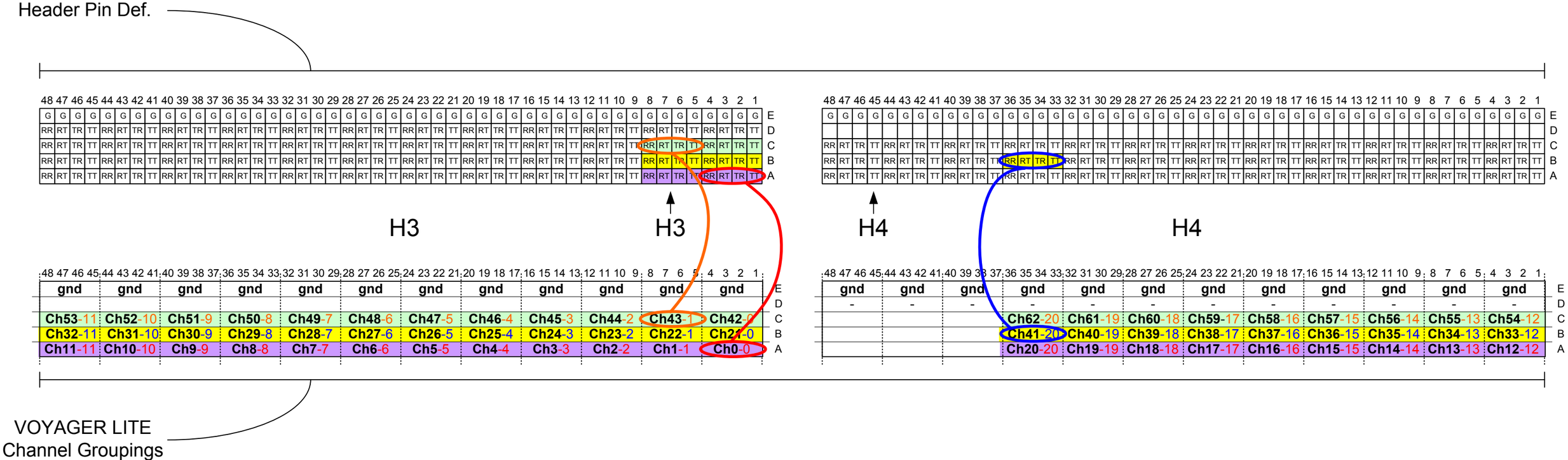
TABLE 2: TRIPLE VOYAGER CHANNEL TO PIN LOCATION CROSS REFERENCE GUIDE

| T1/J1 CHANNEL | XRT86SH328 | DEVICE CHANNEL | HEADER | PIN LOCATION | | | |
|---|---|---|---|---|---|---|---|
| | | | | TTIP | TRING | RTIP | RRING |
| **41** | U3 - Slave 1 | 13 | H4 | B5 | B6 | B7 | B8 |
| **42** | U3 - Slave 1 | 14 | H4 | B9 | B10 | B11 | B12 |
| **43** | U3 - Slave 1 | 15 | H4 | B13 | B14 | B15 | B16 |
| **44** | U3 - Slave 1 | 16 | H4 | B17 | B18 | B19 | B20 |
| **45** | U3 - Slave 1 | 17 | H4 | B21 | B22 | B23 | B24 |
| **46** | U3 - Slave 1 | 18 | H4 | B25 | B26 | B27 | B28 |
| **47** | U3 - Slave 1 | 19 | H4 | B29 | B30 | B31 | B32 |
| **48** | U3 - Slave 1 | 20 | H4 | B33 | B34 | B35 | B36 |
| **49** | U3 - Slave 1 | 21 | H4 | B37 | B38 | B39 | B40 |
| **50** | U3 - Slave 1 | 22 | H4 | B41 | B42 | B43 | B44 |
| **51** | U3 - Slave 1 | 23 | H4 | B45 | B46 | B47 | B48 |
| **52** | U3 - Slave 1 | 24 | H3 | D17 | D18 | D19 | D20 |
| **53** | U3 - Slave 1 | 25 | H3 | D21 | D22 | D23 | D24 |
| **54** | U3 - Slave 1 | 26 | H3 | D25 | D26 | D27 | D28 |
| **55** | U3 - Slave 1 | 27 | H3 | D29 | D30 | D31 | D32 |
| **56** | U4 - Slave 2 | 0 | H3 | C1 | C2 | C3 | C4 |
| **57** | U4 - Slave 2 | 1 | H3 | C5 | C6 | C7 | C8 |
| **58** | U4 - Slave 2 | 2 | H3 | C9 | C10 | C11 | C12 |
| **59** | U4 - Slave 2 | 3 | H3 | C13 | C14 | C15 | C16 |
| **60** | U4 - Slave 2 | 4 | H3 | C17 | C18 | C19 | C20 |
| **61** | U4 - Slave 2 | 5 | H3 | C21 | C22 | C23 | C24 |
| **62** | U4 - Slave 2 | 6 | H3 | C25 | C26 | C27 | C28 |
| **63** | U4 - Slave 2 | 7 | H3 | C29 | C30 | C31 | C32 |
| **64** | U4 - Slave 2 | 8 | H3 | C33 | C34 | C35 | C36 |
| **65** | U4 - Slave 2 | 9 | H3 | C37 | C38 | C39 | C40 |
| **66** | U4 - Slave 2 | 10 | H3 | C41 | C42 | C43 | C44 |
| **67** | U4 - Slave 2 | 11 | H3 | C45 | C46 | C47 | C48 |
| **68** | U4 - Slave 2 | 12 | H4 | C1 | C2 | C3 | C4 |
| **69** | U4 - Slave 2 | 13 | H4 | C5 | C6 | C7 | C8 |
| **70** | U4 - Slave 2 | 14 | H4 | C9 | C10 | C11 | C12 |
| **71** | U4 - Slave 2 | 15 | H4 | C13 | C14 | C15 | C16 |

TABLE 2: TRIPLE VOYAGER CHANNEL TO PIN LOCATION CROSS REFERENCE GUIDE

| T1/J1 CHANNEL | XRT86SH328 | DEVICE CHANNEL | HEADER | PIN LOCATION | | | |
|---|---|---|---|---|---|---|---|
| | | | | TTIP | TRING | RTIP | RRING |
| **72** | U4 - Slave 2 | 16 | H4 | C17 | C18 | C19 | C20 |
| **73** | U4 - Slave 2 | 17 | H4 | C21 | C22 | C23 | C24 |
| **74** | U4 - Slave 2 | 18 | H4 | C25 | C26 | C27 | C28 |
| **75** | U4 - Slave 2 | 19 | H4 | C29 | C30 | C31 | C32 |
| **76** | U4 - Slave 2 | 20 | H4 | C33 | C34 | C35 | C36 |
| **77** | U4 - Slave 2 | 21 | H4 | C37 | C38 | C39 | C40 |
| **78** | U4 - Slave 2 | 22 | H4 | C41 | C42 | C43 | C44 |
| **79** | U4 - Slave 2 | 23 | H4 | C45 | C46 | C47 | C48 |
| **80** | U4 - Slave 2 | 24 | H3 | D33 | D34 | D35 | D36 |
| **81** | U4 - Slave 2 | 25 | H3 | D37 | D38 | D39 | D40 |
| **82** | U4 - Slave 2 | 26 | H3 | D41 | D42 | D43 | D44 |
| **83** | U4 - Slave 2 | 27 | H3 | D45 | D46 | D47 | D48 |

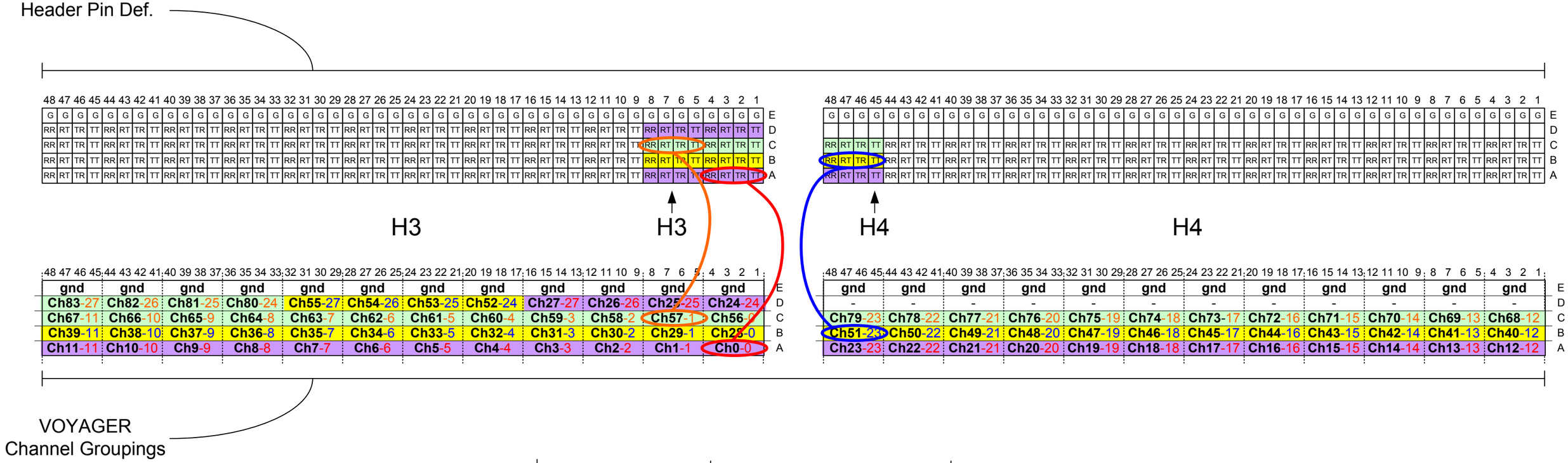
# Line Card E1 Test Interface




| E1 CH # | Device [CH #] | Main Board Device # | Master/Slave |
|---|---|---|---|
| 0 - 20 | A[0:20] | U2 | Master |
| 21 - 41 | B[0:20] | U3 | Slave #1 |
| 42 - 62 | C[0:20] | U4 | Slave #2 |

# Line Card T1/J1 Test Interface

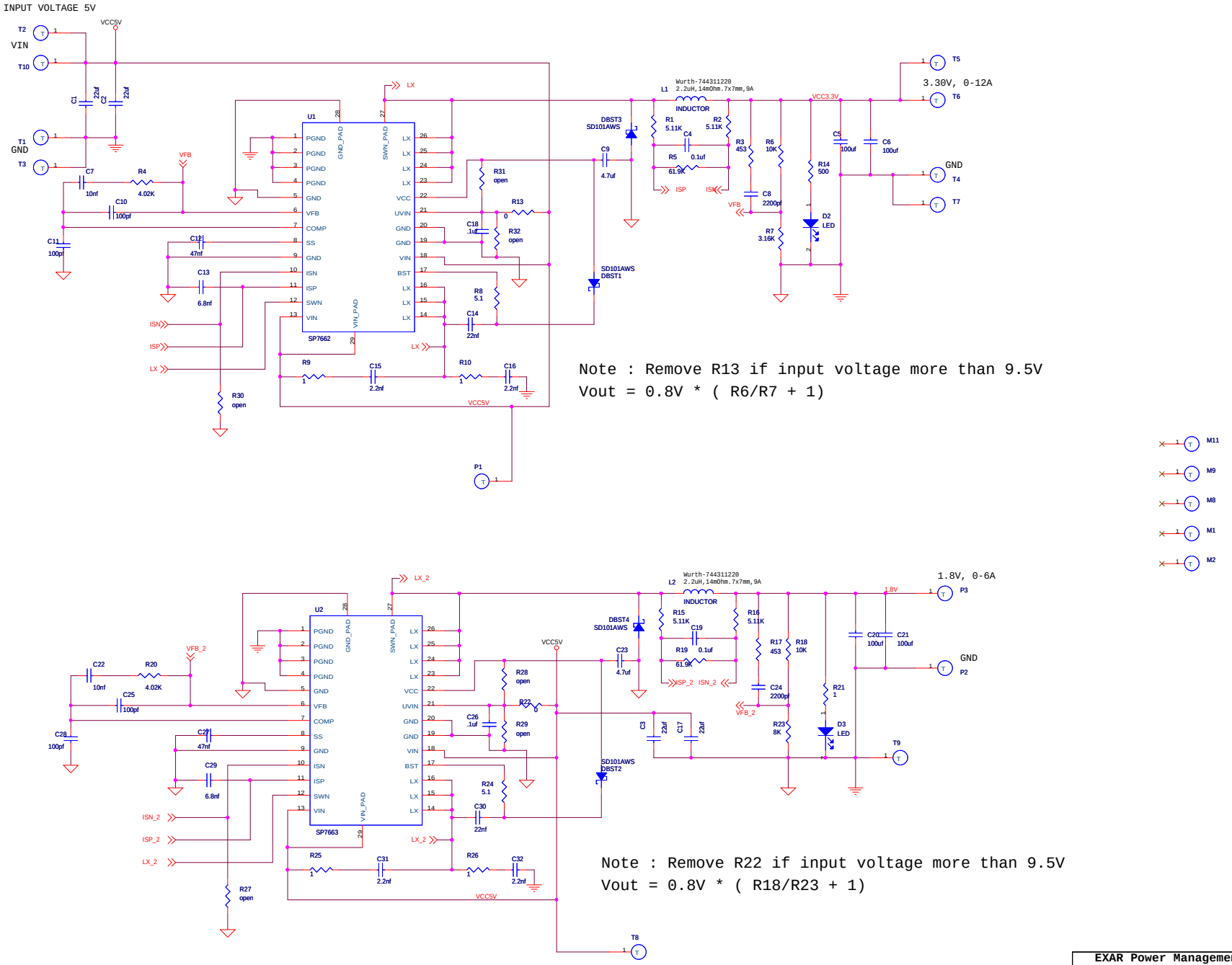
Header Pin Def.




VOYAGER
Channel Groupings

| T1/J1 CH # | Device [CH #] | Main Board Device # | Master/Slave |
|---|---|---|---|
| 0 - 27 | A[0:27] | U2 | Master |
| 28 - 55 | B[0:27] | U3 | Slave #1 |
| 56 - 83 | C[0:27] | U4 | Slave #2 |

# Exar PowerBlox™ Power Supply Reference Design Daughter Card




| EXAR Power Management Solution | | |
|---|---|---|
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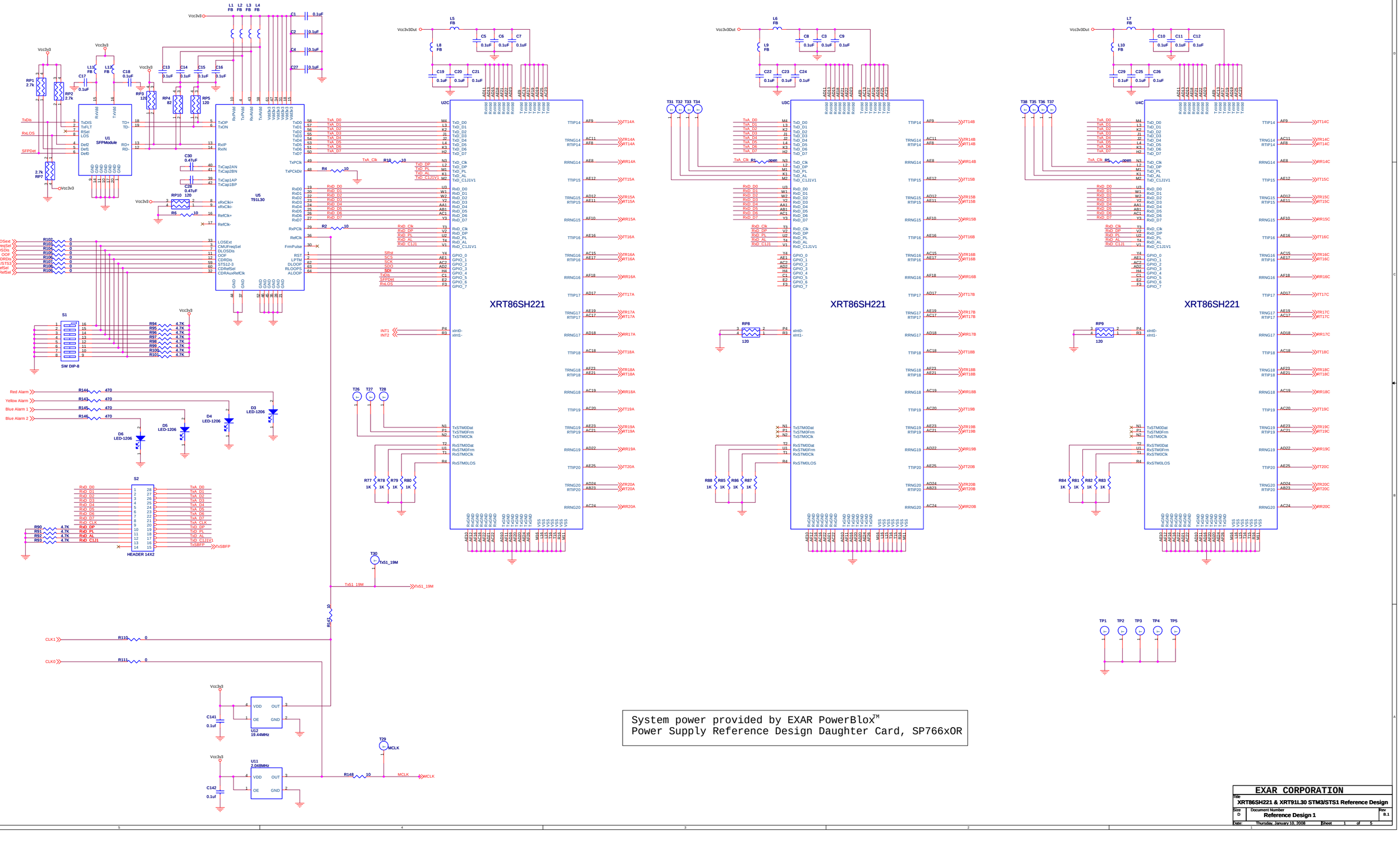
| Size: C | Document Number: SP766xOR | Rev: A |
| Date: Friday, January 11, 2008 | Sheet 1 of 1 | |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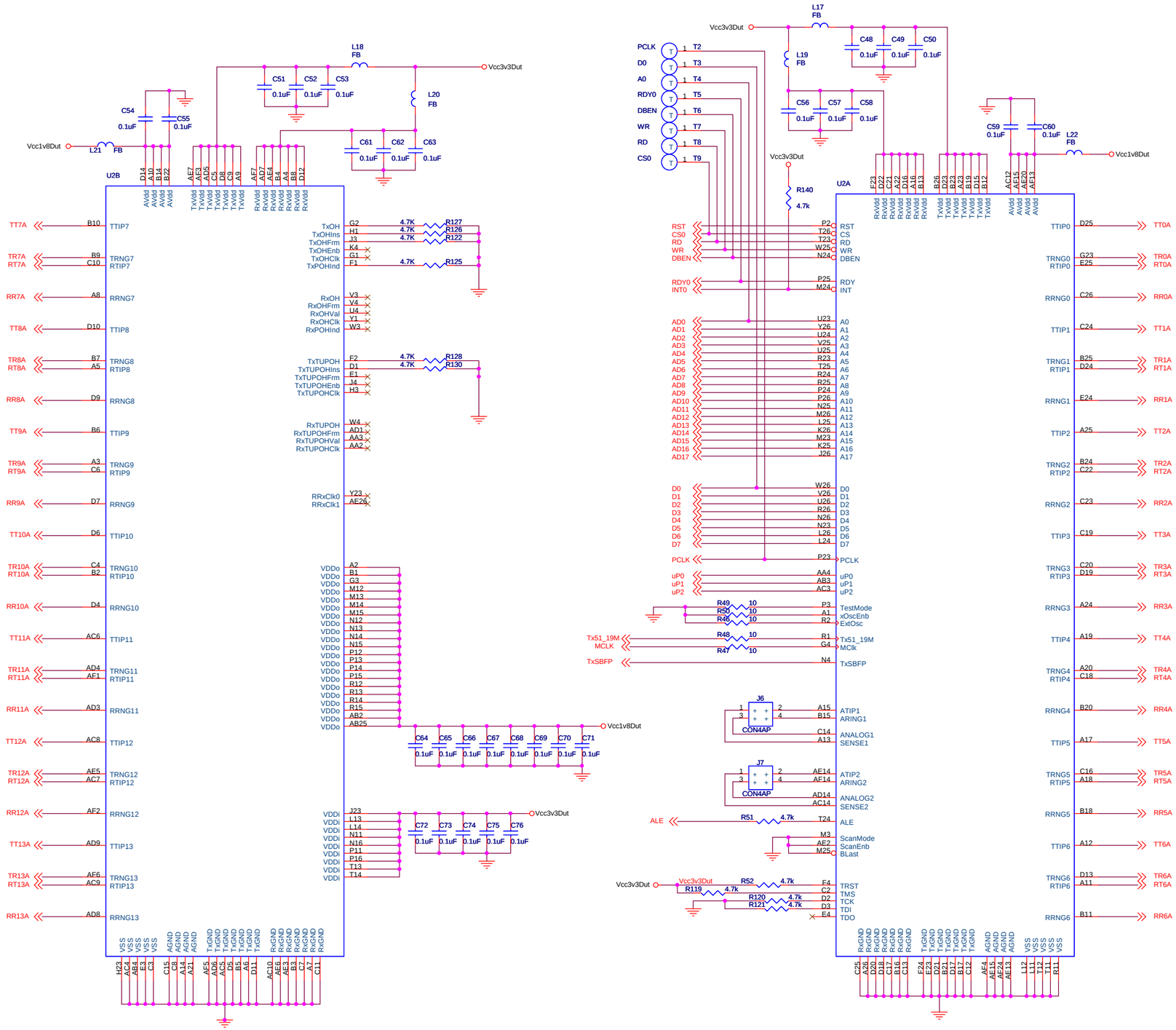
U5 T91L30
U2C
U3C
U4C
XRT86SH221
SW DIP-8
S1
S2
HEADER 14X2
U12 19.44MHz
U11 2.048MHz
LED-1206
System power provided by EXAR PowerBlox™
Power Supply Reference Design Daughter Card, SP766xOR
EXAR CORPORATION
XRT86SH221 & XRT91L30 STM3/STS1 Reference Design
Reference Design 1
Thursday, January 10, 2008




| EXAR CORPORATION | | |
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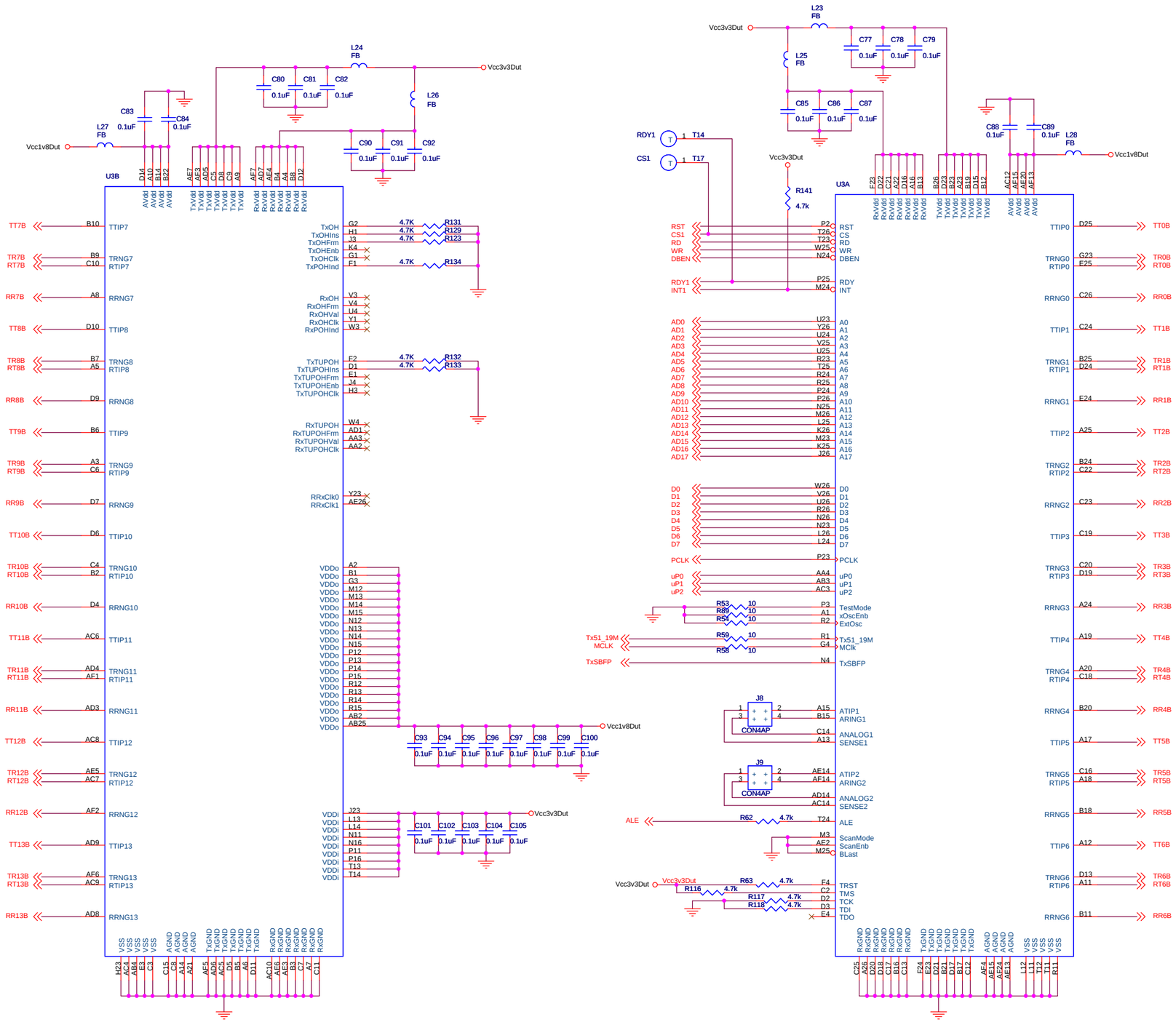
| Size: C | Document Number: Reference Design 1 | Rev: B.1 |
| Date: Thursday, January 10, 2008 | Sheet 2 of 5 | |

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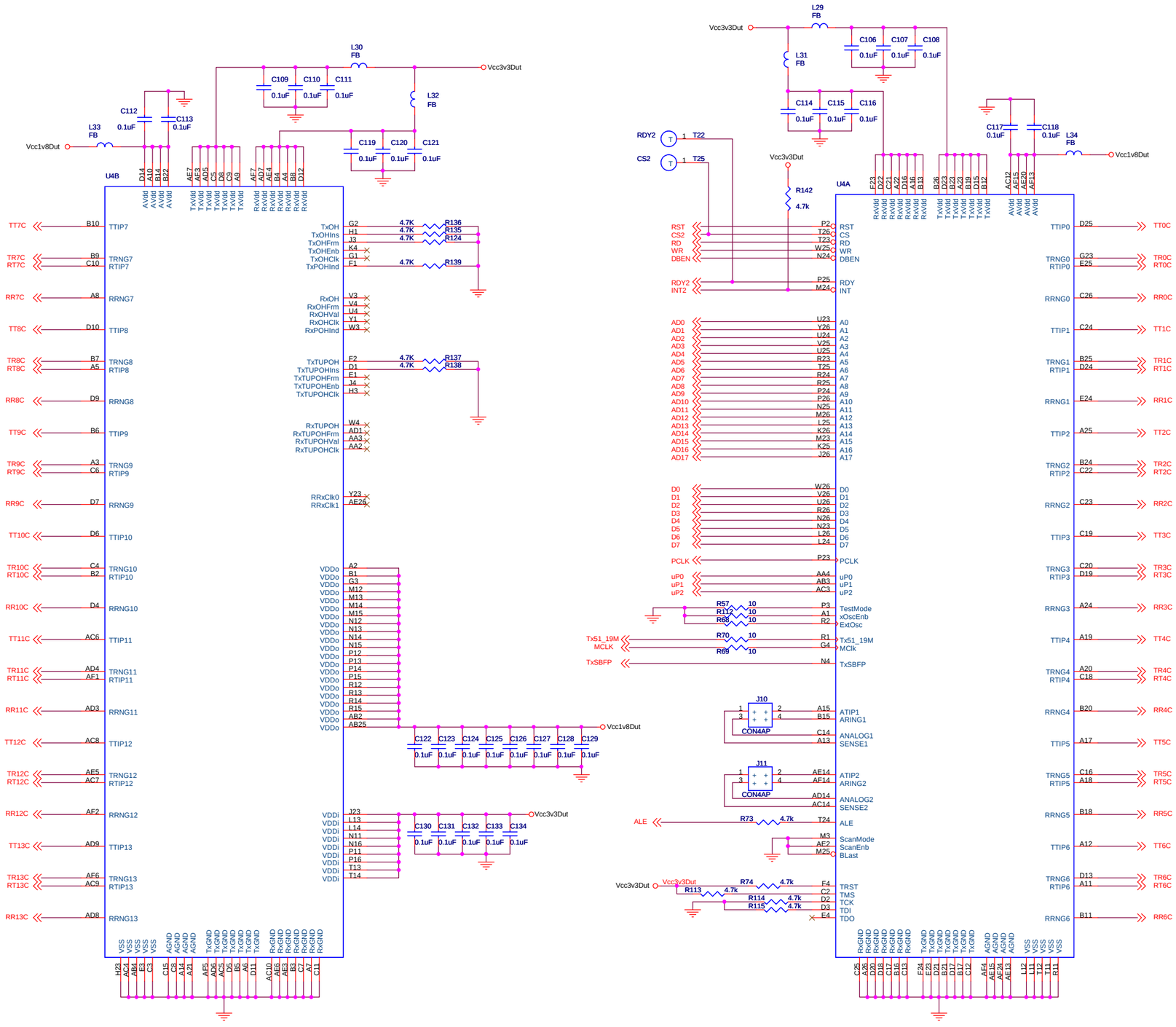
**EXAR CORPORATION**

Title: **XRT86SH221 "Slave 1"**

| Size | Document Number | Rev |
|---|---|---|
| C | Reference Design 1 | B.1 |

Date: Thursday, January 10, 2008 Sheet 3 of 5

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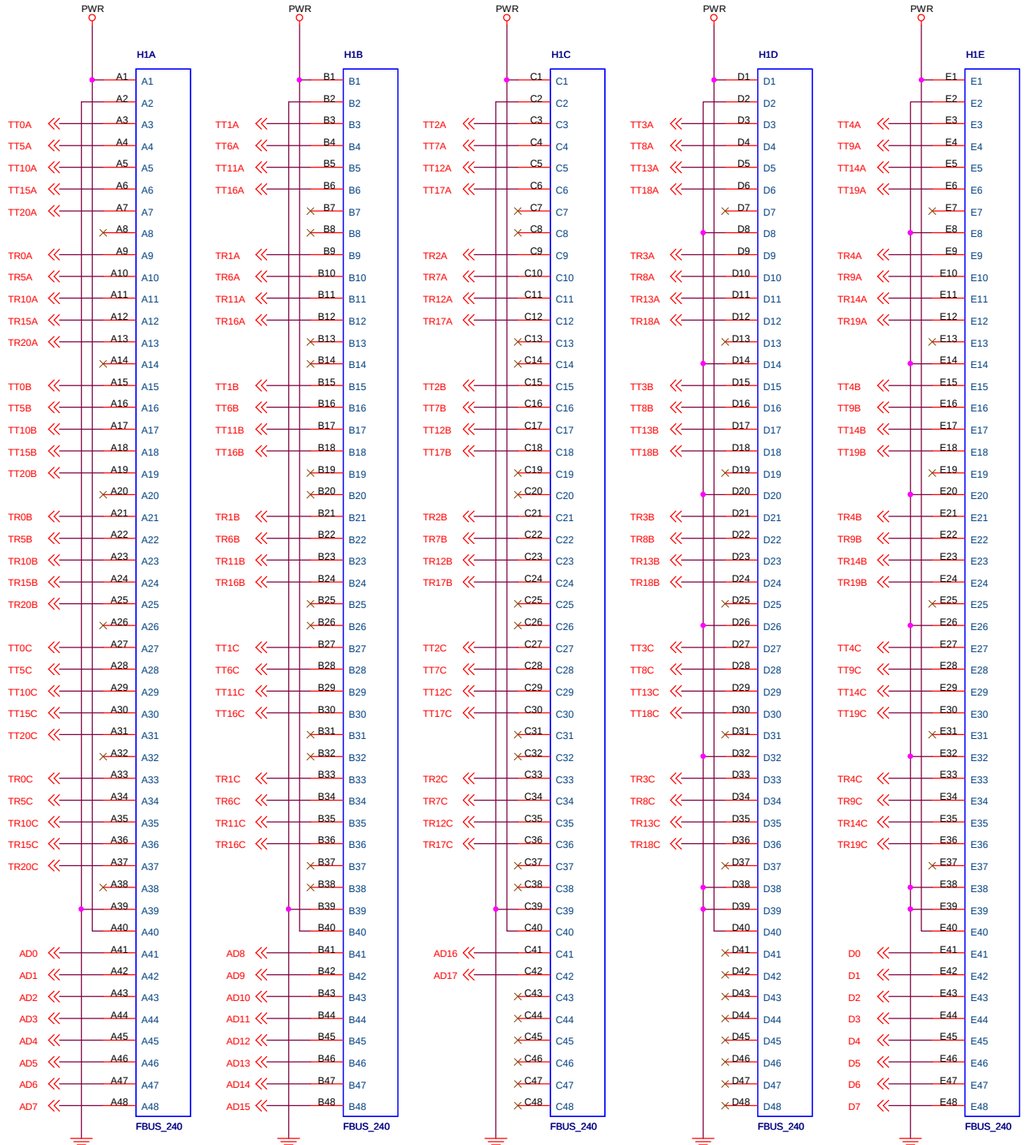
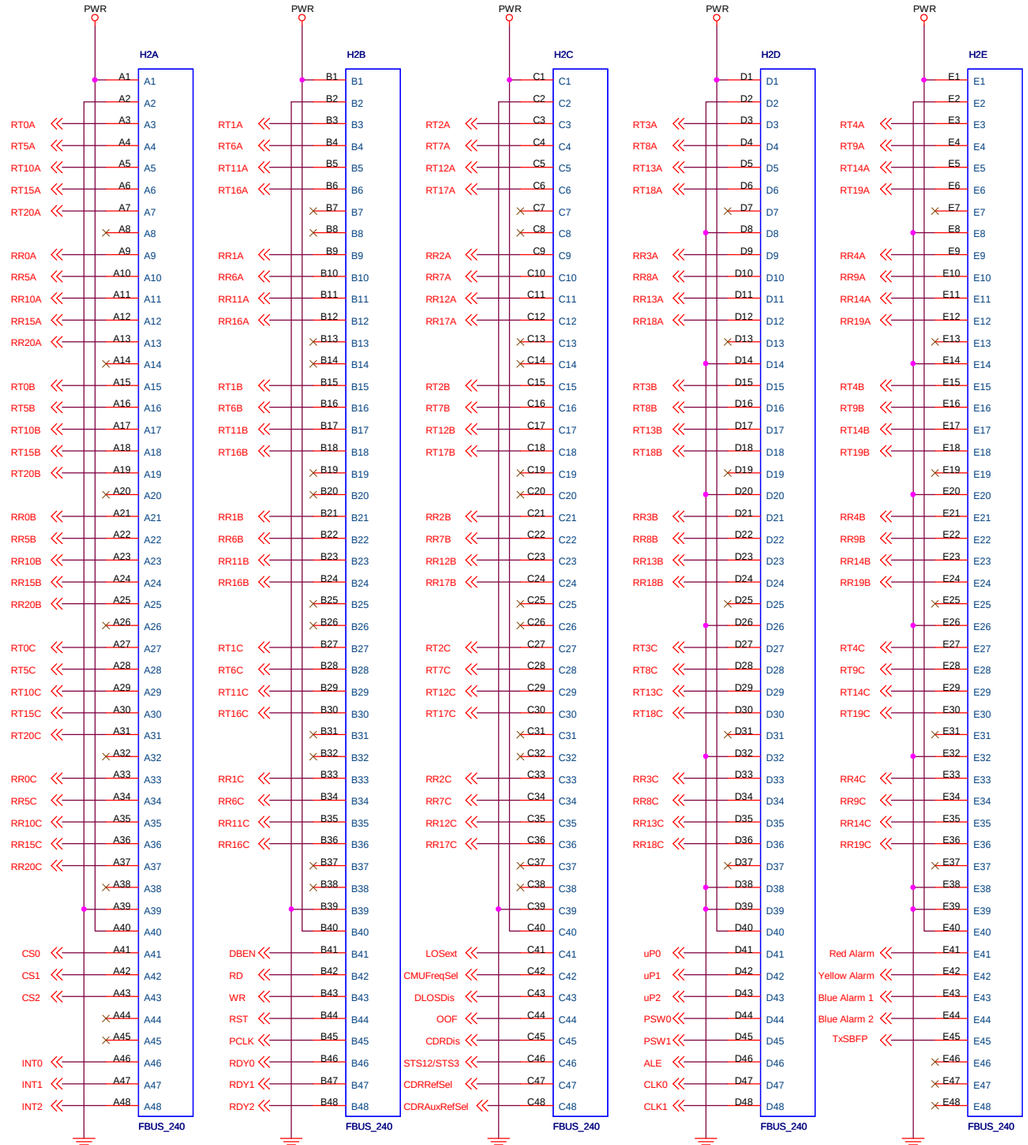
| Title | **XRT86SH221 "Slave 2"** | | |
| Size C | Document Number **Reference Design 1** | | Rev B.1 |
| Date: Thursday, January 10, 2008 | Sheet 4 of 5 | | |

# Transmitt




# Receive




| EXAR CORPORATION | | | |
|---|---|---|---|
| Title: Back Plane Connectors | | | |
| Size: C | Document Number: Reference Design 1 | | Rev: B.1 |
| Date: Thursday, January 10, 2008 | Sheet 5 of 5 | | |

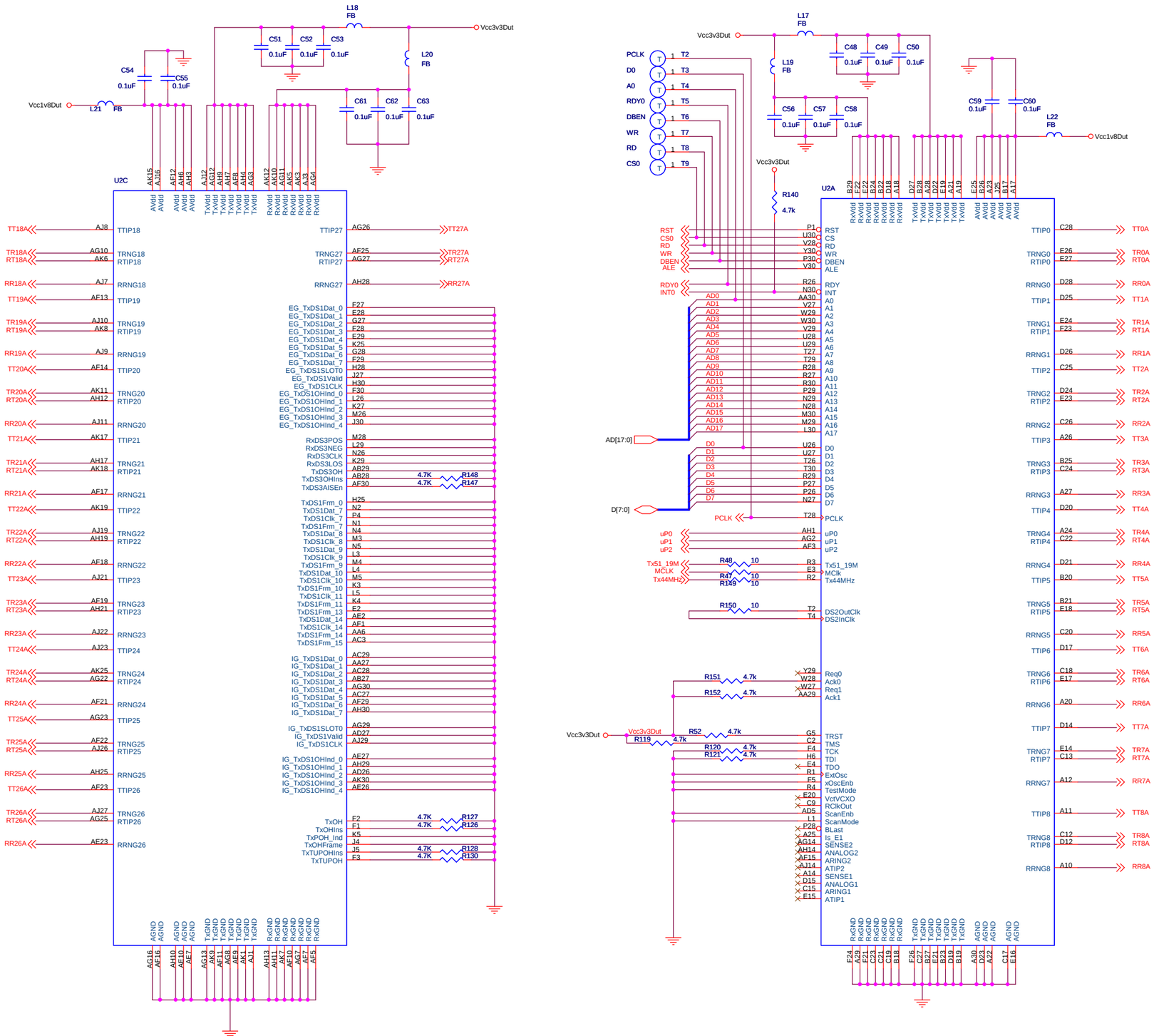
Master Receive
OverHead Port

Slave 1 Transmit
OverHead Port

System power provided by EXAR PowerBlox™
Power Supply Reference Design Daughter Card, SP766xOR

**EXAR Experience our Connectivity**

| | | |
|---|---|---|
| Title: XRT86SH328 & XRT91L30 STM3/STS1 Reference Design | | |
| Size: D | Document Number: ORION Reference Design 2b | Rev: B.1 |
| Date: Thursday, January 10, 2008 | Sheet 1 of 6 | |




| | |
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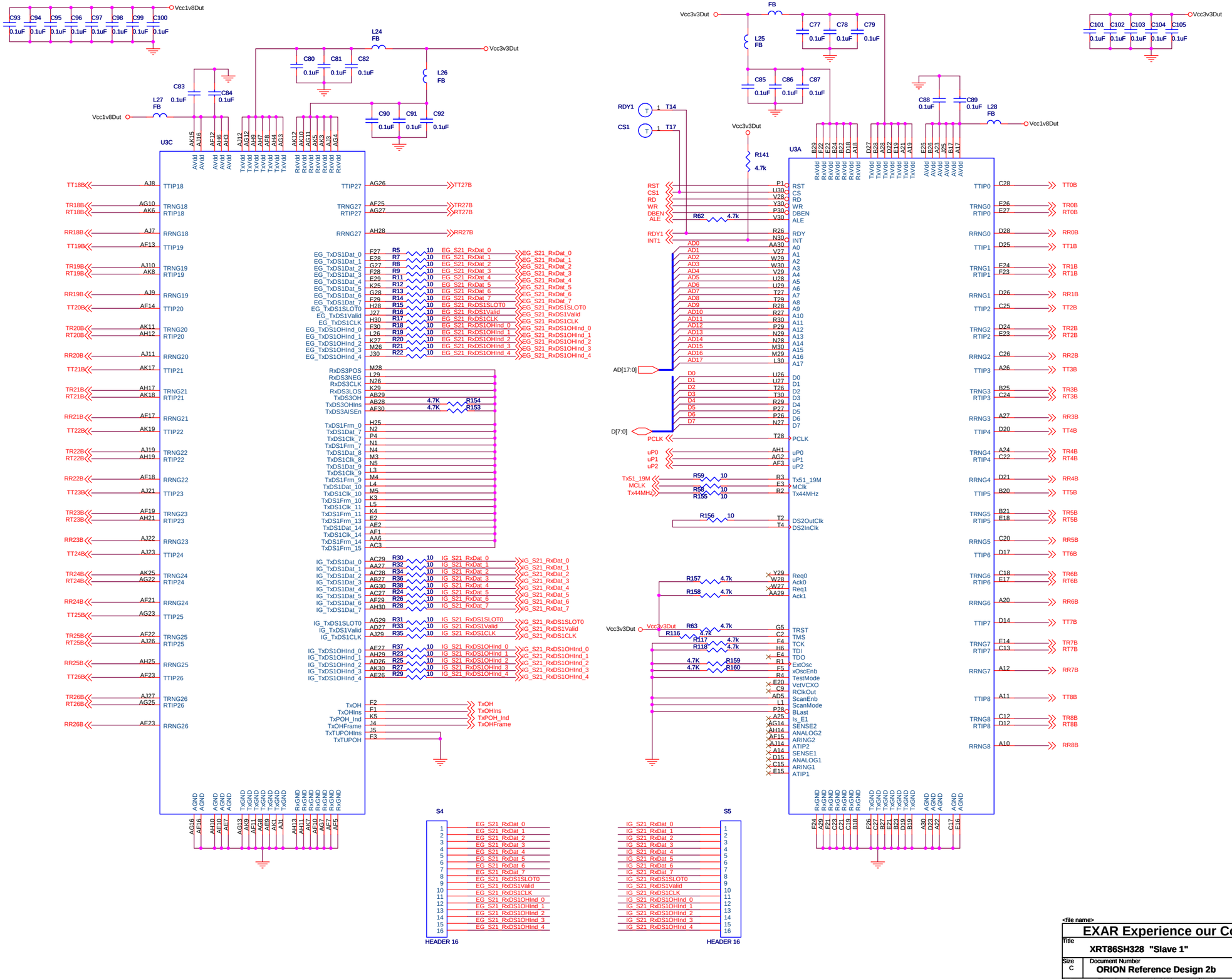
| Title | EXAR Experience our Connectivity |
| | XRT86SH328 "Master" |
| Size | C |
| Document Number | ORION Reference Design 2b |
| Rev | B.1 |
| Date: | Thursday, January 10, 2008 |
| Sheet | 2 of 6 |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RST
CS
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DS2InClk
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Ack0
Req1
Ack1
TRST
TMS
TCK
TDI
TDO
ExtOsc
xOscEnb
TestMode
VctVCXO
RClkOut
ScanEnb
ScanMode
BLast
Is_E1
SENSE2
ANALOG2
ARING2
ATIP2
SENSE1
ANALOG1
ARING1
ATIP1
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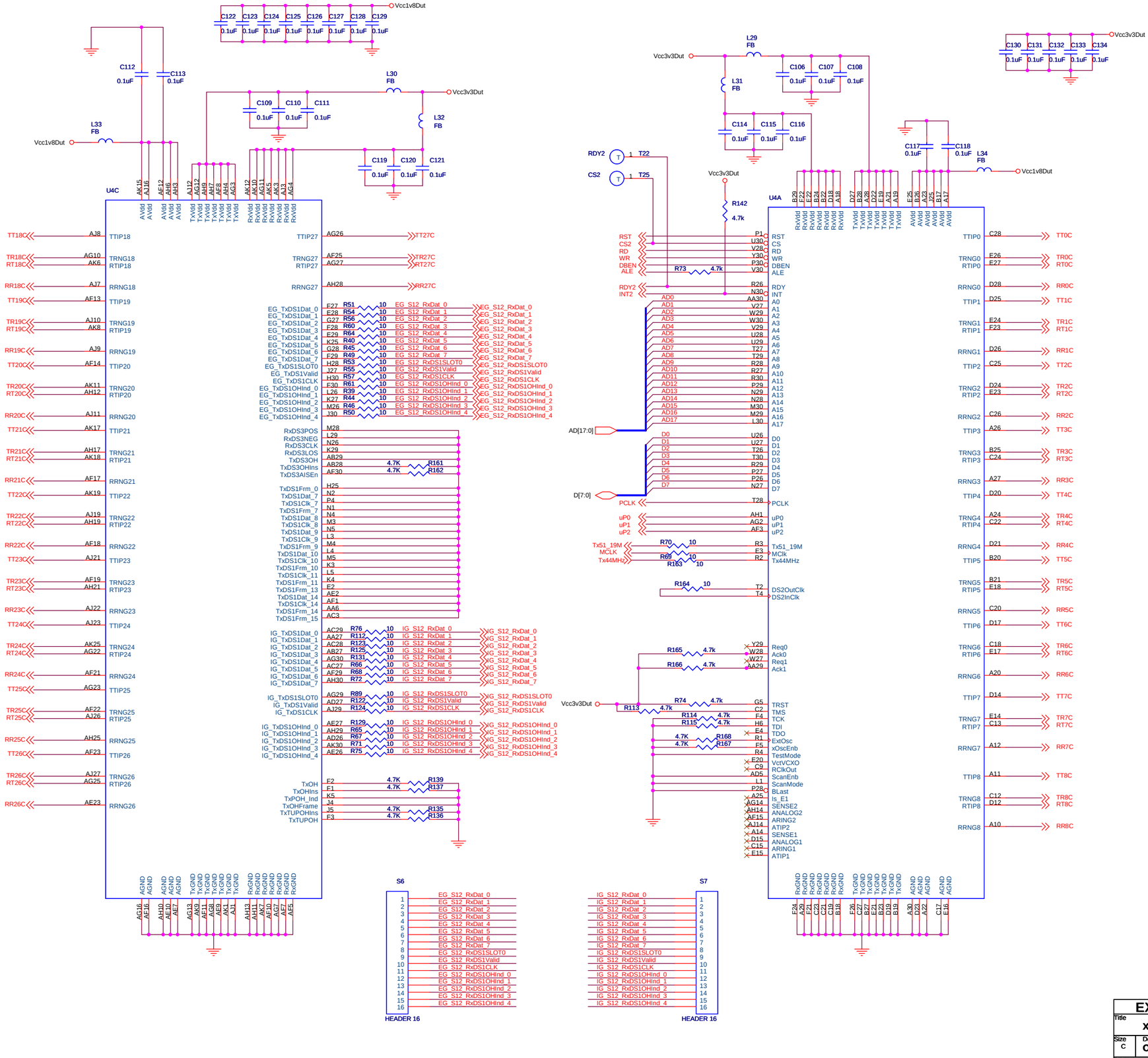
XRT86SH328 "Slave 1"
Size C
Document Number
ORION Reference Design 2b
Rev B.1
Date: Thursday, January 10, 2008
Sheet 3 of 6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TR18C AG10 TRNG18
RT18C AK6 RTIP18
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EG_TxDS1Dat_2 G27 R56 10 EG_S12_RxDat_2 EG_S12_RxDat_2
EG_TxDS1Dat_3 F28 R60 10 EG_S12_RxDat_3 EG_S12_RxDat_3
EG_TxDS1Dat_4 E29 R64 10 EG_S12_RxDat_4 EG_S12_RxDat_4
EG_TxDS1Dat_5 K25 R40 10 EG_S12_RxDat_5 EG_S12_RxDat_5
EG_TxDS1Dat_6 G28 R45 10 EG_S12_RxDat_6 EG_S12_RxDat_6
EG_TxDS1Dat_7 F29 R49 10 EG_S12_RxDat_7 EG_S12_RxDat_7
EG_TxDS1SLOT0 H28 R53 10 EG_S12_RxDS1SLOT0 EG_S12_RxDS1SLOT0
EG_TxDS1Valid J27 R55 10 EG_S12_RxDS1Valid EG_S12_RxDS1Valid
EG_TxDS1CLK H30 R57 10 EG_S12_RxDS1CLK EG_S12_RxDS1CLK
EG_TxDS1OHInd_0 F30 R61 10 EG_S12_RxDS1OHInd_0 EG_S12_RxDS1OHInd_0
EG_TxDS1OHInd_1 L26 R39 10 EG_S12_RxDS1OHInd_1 EG_S12_RxDS1OHInd_1
EG_TxDS1OHInd_2 K27 R44 10 EG_S12_RxDS1OHInd_2 EG_S12_RxDS1OHInd_2
EG_TxDS1OHInd_3 M26 R46 10 EG_S12_RxDS1OHInd_3 EG_S12_RxDS1OHInd_3
EG_TxDS1OHInd_4 J30 R50 10 EG_S12_RxDS1OHInd_4 EG_S12_RxDS1OHInd_4
RxDS3POS M28
RxDS3NEG L29
RxDS3CLK N26
RxDS3LOS K29
TxDS3OH AB29
TxDS3OHIns AB28 4.7K R161
TxDS3AISEn AF30 4.7K R162
TxDS1Frm_0 H25
TxDS1Dat_7 N2
TxDS1Clk_7 P4
TxDS1Frm_7 N1
TxDS1Dat_8 N4
TxDS1Clk_8 M3
TxDS1Dat_9 N5
TxDS1Clk_9 L3
TxDS1Frm_9 M4
TxDS1Dat_10 L4
TxDS1Clk_10 M5
TxDS1Frm_10 K3
TxDS1Clk_11 L5
TxDS1Frm_11 K4
TxDS1Frm_13 E2
TxDS1Dat_14 AE2
TxDS1Clk_14 AF1
TxDS1Frm_14 AA6
TxDS1Frm_15 AC3
IG_TxDS1Dat_0 AC29 R76 10 IG_S12_RxDat_0 IG_S12_RxDat_0
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IG_TxDS1Dat_2 AC28 R123 10 IG_S12_RxDat_2 IG_S12_RxDat_2
IG_TxDS1Dat_3 AB27 R125 10 IG_S12_RxDat_3 IG_S12_RxDat_3
IG_TxDS1Dat_4 AG30 R131 10 IG_S12_RxDat_4 IG_S12_RxDat_4
IG_TxDS1Dat_5 AC27 R66 10 IG_S12_RxDat_5 IG_S12_RxDat_5
IG_TxDS1Dat_6 AF29 R68 10 IG_S12_RxDat_6 IG_S12_RxDat_6
IG_TxDS1Dat_7 AH30 R72 10 IG_S12_RxDat_7 IG_S12_RxDat_7
IG_TxDS1SLOT0 AG29 R89 10 IG_S12_RxDS1SLOT0 IG_S12_RxDS1SLOT0
IG_TxDS1Valid AD27 R122 10 IG_S12_RxDS1Valid IG_S12_RxDS1Valid
IG_TxDS1CLK AJ29 R124 10 IG_S12_RxDS1CLK IG_S12_RxDS1CLK
IG_TxDS1OHInd_0 AE27 R129 10 IG_S12_RxDS1OHInd_0 IG_S12_RxDS1OHInd_0
IG_TxDS1OHInd_1 AH29 R65 10 IG_S12_RxDS1OHInd_1 IG_S12_RxDS1OHInd_1
IG_TxDS1OHInd_2 AD26 R67 10 IG_S12_RxDS1OHInd_2 IG_S12_RxDS1OHInd_2
IG_TxDS1OHInd_3 AK30 R71 10 IG_S12_RxDS1OHInd_3 IG_S12_RxDS1OHInd_3
IG_TxDS1OHInd_4 AE26 R75 10 IG_S12_RxDS1OHInd_4 IG_S12_RxDS1OHInd_4
TxOH F2 4.7K R139
TxOHIns F1 4.7K R137
TxPOH_Ind K5
TxOHFrame J4
TxTUPOHIns J5 4.7K R135
TxTUPOH F3 4.7K R136
AGND AGND AGND AGND AGND
TxGND TxGND TxGND TxGND TxGND TxGND TxGND
RxGND RxGND RxGND RxGND RxGND RxGND RxGND
AG16 AF16 AH10 AE10 AE7 AG13 AK4 AF11 AG8 AE9 AK1 AJ1 AH13 AH11 AK7 AF10 AG7 AE7 AE5
S6
EG_S12_RxDat_0
EG_S12_RxDat_1
EG_S12_RxDat_2
EG_S12_RxDat_3
EG_S12_RxDat_4
EG_S12_RxDat_5
EG_S12_RxDat_6
EG_S12_RxDat_7
EG_S12_RxDS1SLOT0
EG_S12_RxDS1Valid
EG_S12_RxDS1CLK
EG_S12_RxDS1OHInd_0
EG_S12_RxDS1OHInd_1
EG_S12_RxDS1OHInd_2
EG_S12_RxDS1OHInd_3
EG_S12_RxDS1OHInd_4
HEADER 16
S7
IG_S12_RxDat_0
IG_S12_RxDat_1
IG_S12_RxDat_2
IG_S12_RxDat_3
IG_S12_RxDat_4
IG_S12_RxDat_5
IG_S12_RxDat_6
IG_S12_RxDat_7
IG_S12_RxDS1SLOT0
IG_S12_RxDS1Valid
IG_S12_RxDS1CLK
IG_S12_RxDS1OHInd_0
IG_S12_RxDS1OHInd_1
IG_S12_RxDS1OHInd_2
IG_S12_RxDS1OHInd_3
IG_S12_RxDS1OHInd_4
HEADER 16
Vcc3v3Dut
L29 FB
L31 FB
C106 C107 C108 0.1uF
C114 C115 C116 0.1uF
C130 C131 C132 C133 C134 0.1uF
C117 0.1uF
C118 0.1uF
L34 FB
Vcc1v8Dut
RDY2
CS2
T22
T25
R142 4.7k
U4A
B29 F22 E22 B24 B23 D18 A18
RxVdd RxVdd RxVdd RxVdd RxVdd RxVdd RxVdd
L27 B28 A28 D22 E19 A21 A19
TxVdd TxVdd TxVdd TxVdd TxVdd TxVdd TxVdd
E25 B26 A26 A23 J25 B17 A17
AVdd AVdd AVdd AVdd AVdd AVdd AVdd
RST P1 RST
CS2 U30 CS
RD V28 RD
WR Y30 WR
DBEN P30 DBEN
ALE V30 ALE
R73 4.7k
RDY2 R26 RDY
INT2 N30 INT
AD0 AA30 A0
AD1 V27 A1
AD2 W29 A2
AD3 W30 A3
AD4 V29 A4
AD5 U28 A5
AD6 U29 A6
AD7 T27 A7
AD8 T29 A8
AD9 R28 A9
AD10 R27 A10
AD11 R30 A11
AD12 P29 A12
AD13 N29 A13
AD14 N28 A14
AD15 M30 A15
AD16 M29 A16
AD17 L30 A17
AD[17:0]
D0 U26 D0
D1 U27 D1
D2 T26 D2
D3 T30 D3
D4 R29 D4
D5 P27 D5
D6 P26 D6
D7 N27 D7
D[7:0]
PCLK T28 PCLK
uP0 AH1 uP0
uP1 AG2 uP1
uP2 AF3 uP2
Tx51_19M R70 10 R3 Tx51_19M
MCLK E3 MClk
Tx44MHz R69 10 R2 Tx44MHz
R183 10
R164 10 T2 DS2OutClk
T4 DS2InClk
R165 4.7k Y29 Req0
R166 4.7k W28 Ack0
W27 Req1
AA29 Ack1
Vcc3v3Dut
R113 4.7k
R74 4.7k G5 TRST
C2 TMS
R114 4.7k F4 TCK
R115 4.7k H6 TDI
4.7k R168 E4 TDO
4.7k R167 R1 ExtOsc
F5 xOscEnb
R4 TestMode
E20 VctVCXO
C9 RClkOut
AD5 ScanEnb
L1 ScanMode
P28 BLast
A25 Is_E1
AG14 SENSE2
AH14 ANALOG2
AF15 ARING2
AJ14 ATIP2
A14 SENSE1
D15 ANALOG1
C15 ARING1
E15 ATIP1
TTIP0 C28 TT0C
TRNG0 E26 TR0C
RTIP0 E27 RT0C
RRNG0 D28 RR0C
TTIP1 D25 TT1C
TRNG1 E24 TR1C
RTIP1 F23 RT1C
RRNG1 D26 RR1C
TTIP2 C25 TT2C
TRNG2 D24 TR2C
RTIP2 E23 RT2C
RRNG2 C26 RR2C
TTIP3 A26 TT3C
TRNG3 B25 TR3C
RTIP3 C24 RT3C
RRNG3 A27 RR3C
TTIP4 D20 TT4C
TRNG4 A24 TR4C
RTIP4 C22 RT4C
RRNG4 D21 RR4C
TTIP5 B20 TT5C
TRNG5 B21 TR5C
RTIP5 E18 RT5C
RRNG5 C20 RR5C
TTIP6 D17 TT6C
TRNG6 C18 TR6C
RTIP6 E17 RT6C
RRNG6 A20 RR6C
TTIP7 D14 TT7C
TRNG7 E14 TR7C
RTIP7 C13 RT7C
RRNG7 A12 RR7C
TTIP8 A11 TT8C
TRNG8 C12 TR8C
RTIP8 D12 RT8C
RRNG8 A10 RR8C
RXGND RXGND RXGND RXGND RXGND RXGND RXGND
TXGND TXGND TXGND TXGND TXGND TXGND TXGND
AGND AGND AGND AGND AGND
F24 A29 F21 C23 C21 C19 B18 F26 C27 B27 E21 B23 B19 B19 A30 D23 A22 C17 E16
EXAR Experience our Connectivity
Title
XRT86SH328 "Slave 2"
Size C
Document Number
ORION Reference Design 2b
Rev B.1
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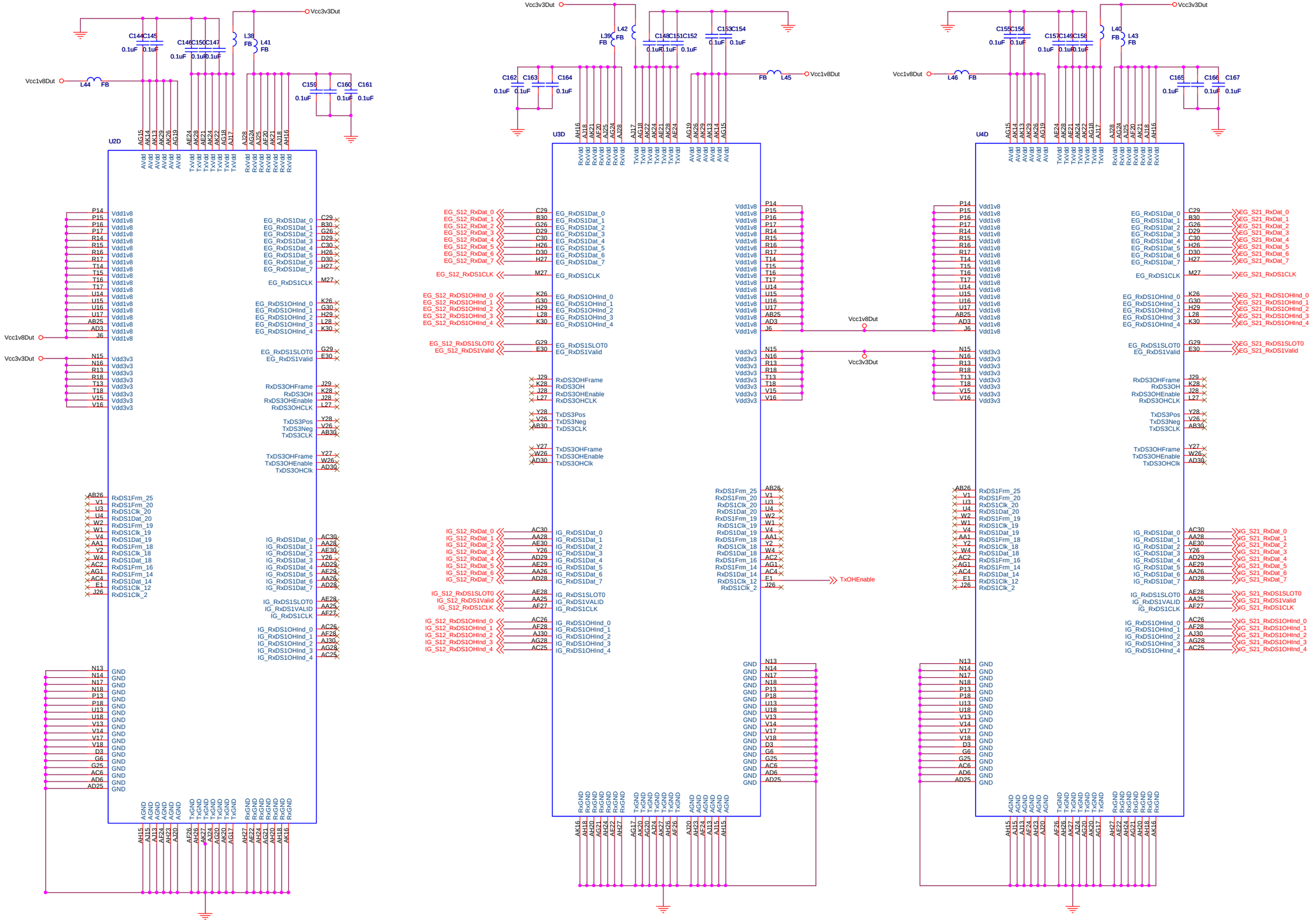


# EXAR Experience our Connectivity

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| Title: Voyager (XRT86SH328) - misc | | |
| Size: C | Document Number: ORION Reference Design 2b | Rev: B.1 |
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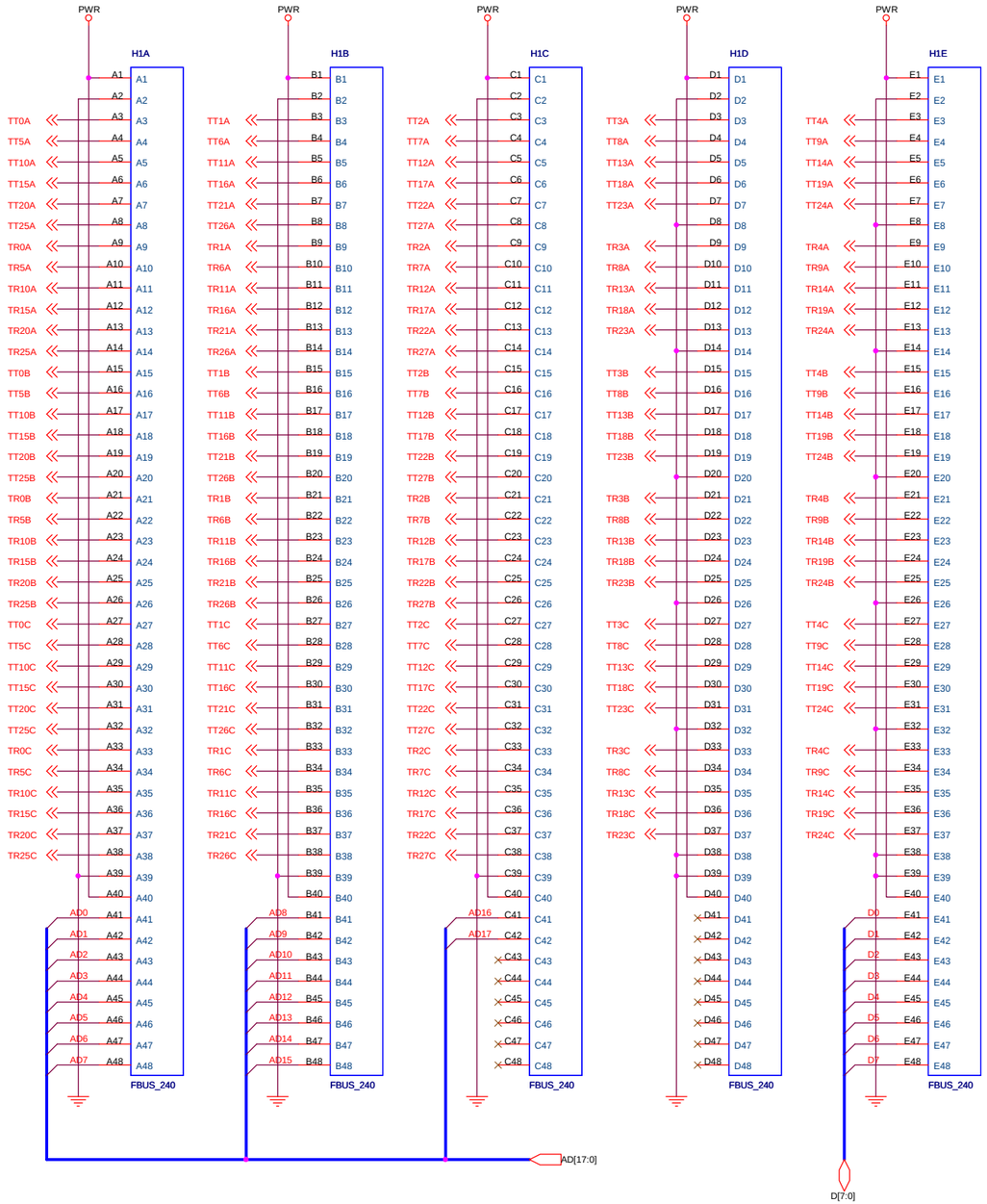
# Transmit

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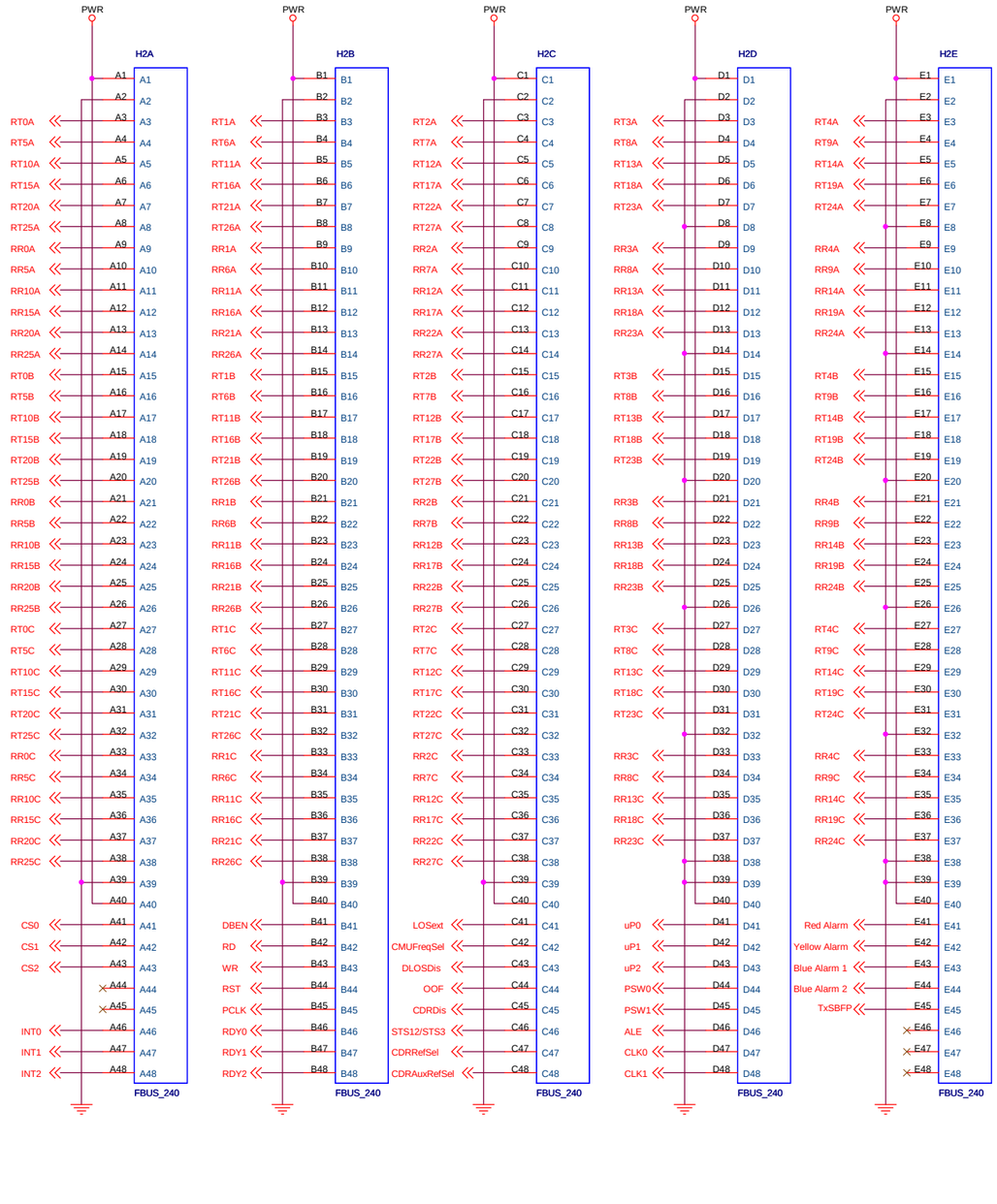


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| Title: Back Plane Connectors | | |
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| Date: Thursday, January 10, 2008 | Sheet 6 of 6 | |